EE 330
Lecture 10

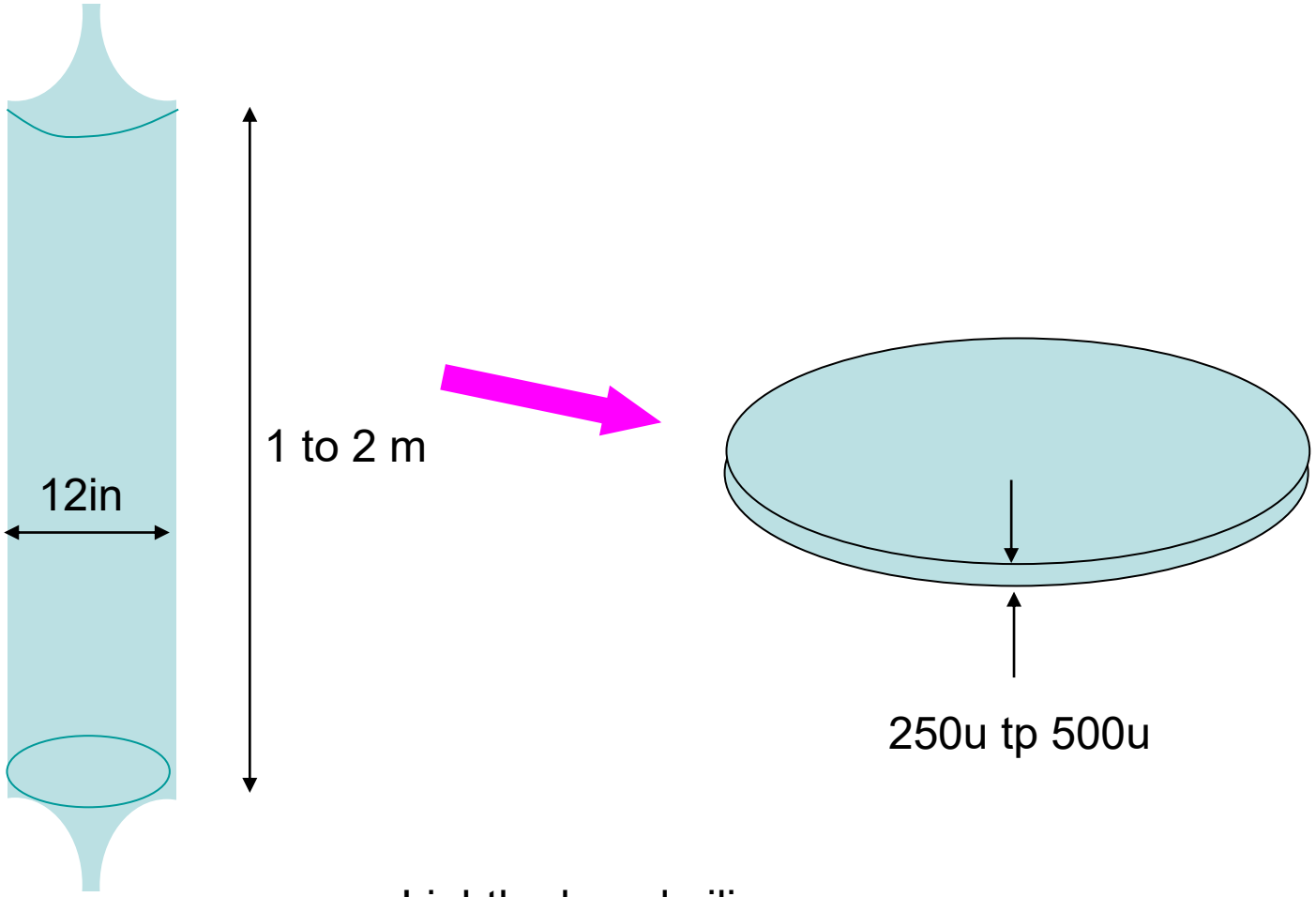
IC Fabrication Technology

- Deposition
- Ion Implantation
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Planarization
- Contacts, Interconnect, and Metallization

Exam 1	Friday Sept 23	
Exam 2	Friday Oct 21	
Exam 3	Friday Nov 13	
Final	Tuesday Dec 13	12:00 – 2:00 p.m.

Review from Last Time

Crystal Preparation



Some predict newer FABs to be at 450mm (18in) by 2020 but appears to be uncertain whether it will ever happen

Lightly-doped silicon
Excellent crystalline structure

Review from Last Time

Masking

Mask Features

Review from Last Time

Photolithographic Process

- Photoresist
  - Viscous Liquid
  - Uniform Application Critical (spinner)
  - Baked to harden
  - Approx 1u thick
  - Non-Selective
  - Types
    - Negative – unexposed material removed when developed
    - Positive-exposed material removed when developed
    - Thickness about 450nm in 90nm process (ITRS 2007 Litho)
- Exposure
  - Projection through reticle with stepper (scanners becoming popular)
  - Alignment is critical !!
  - E-Bean Exposures
    - Eliminate need fro reticle
    - Capacity very small

Stepper: Optics fixed, wafer steps in fixed increments
Scanner: Wafer steps in fixed increments and during exposure both optics and wafer are moved to increase effective reticle size

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Deposition

- Application of something to the surface of the silicon wafer or substrate
  - Layers 15A to 20u thick
- Methods
  - Physical Vapor Deposition (nonselective)
    - Evaporation/Condensation
    - Sputtering (better host integrity)
  - Chemical Vapor Deposition (nonselective)
    - Reaction of 2 or more gases with solid precipitate
    - Reduction by heating creates solid precipitate (pyrolytic)
  - Screening (selective)
    - For thick films
    - Low Tech, not widely used today

Deposition

Example: Chemical Vapor Deposition

Silane (SiH_4) is a gas (toxic and spontaneously combustible in air) at room temperature but breaks down into Si and H_2 above 400^{o}C so can be used to deposit Si.

$$S_iH_4 \rightarrow S_i + 2H_2$$

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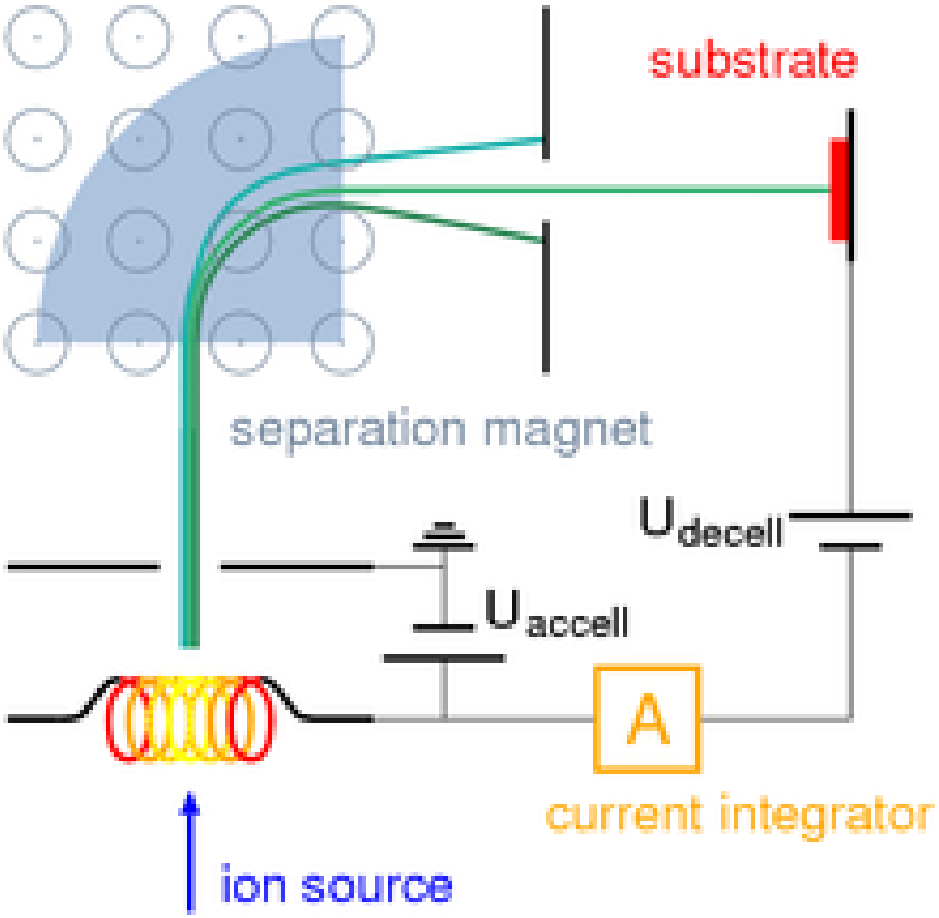
Ion Implantation

Application of impurities into the surface of the silicon wafer or substrate

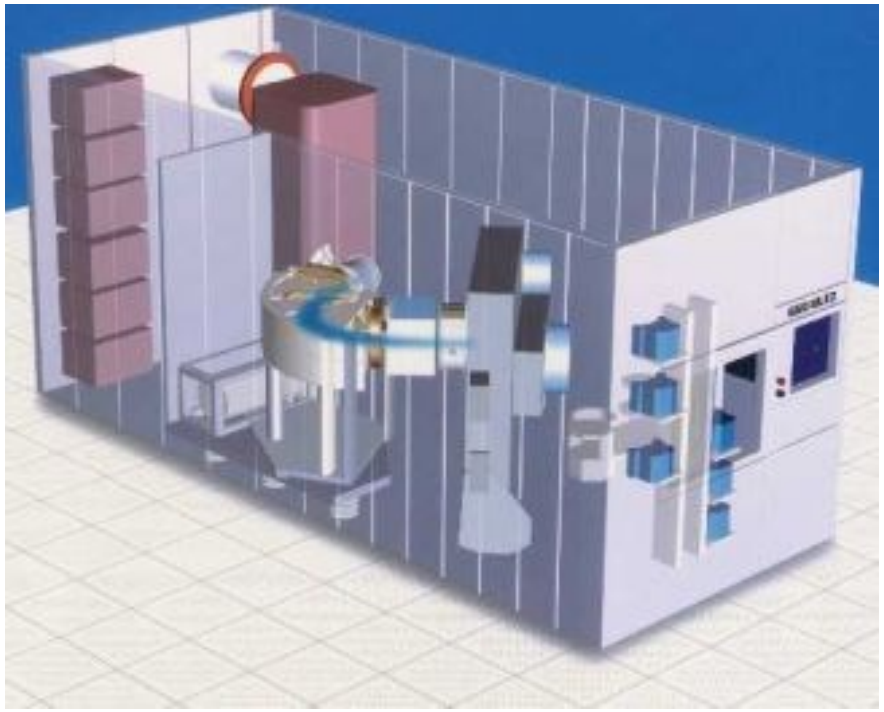
- Individual atoms are first ionized (so they can be accelerated)
- Impinge on the surface and burry themselves into the upper layers
- Often very shallow but with high enough energy can go modestly deep
- Causes damage to target on impact
- Annealing heals most of the damage
- Very precise control of impurity numbers is possible
- Very high energy required
- High-end implanters considered key technology for national security

Ion Implantation Process



From: https://en.wikipedia.org/wiki/Ion_implantation

Ion Implanter



From http://www.casetechnology.com/implanter

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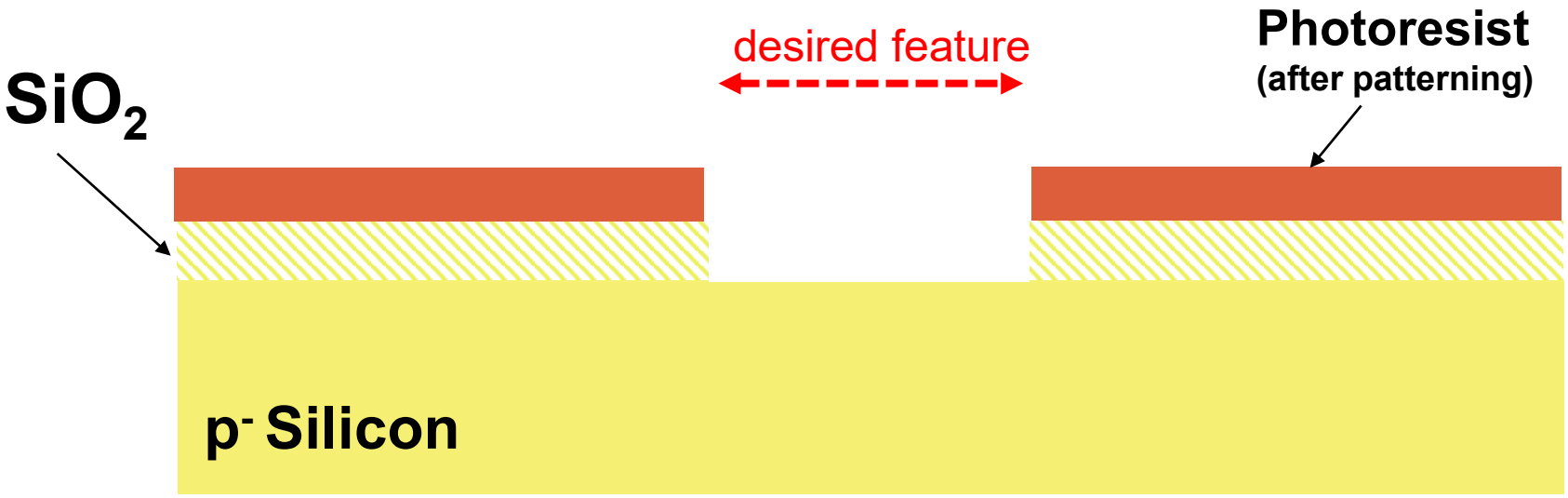
Etching

Selective Removal of Unwanted Materials

- Wet Etch
  - Inexpensive but under-cutting a problem
- Dry Etch
  - Often termed ion etch or plasma etch

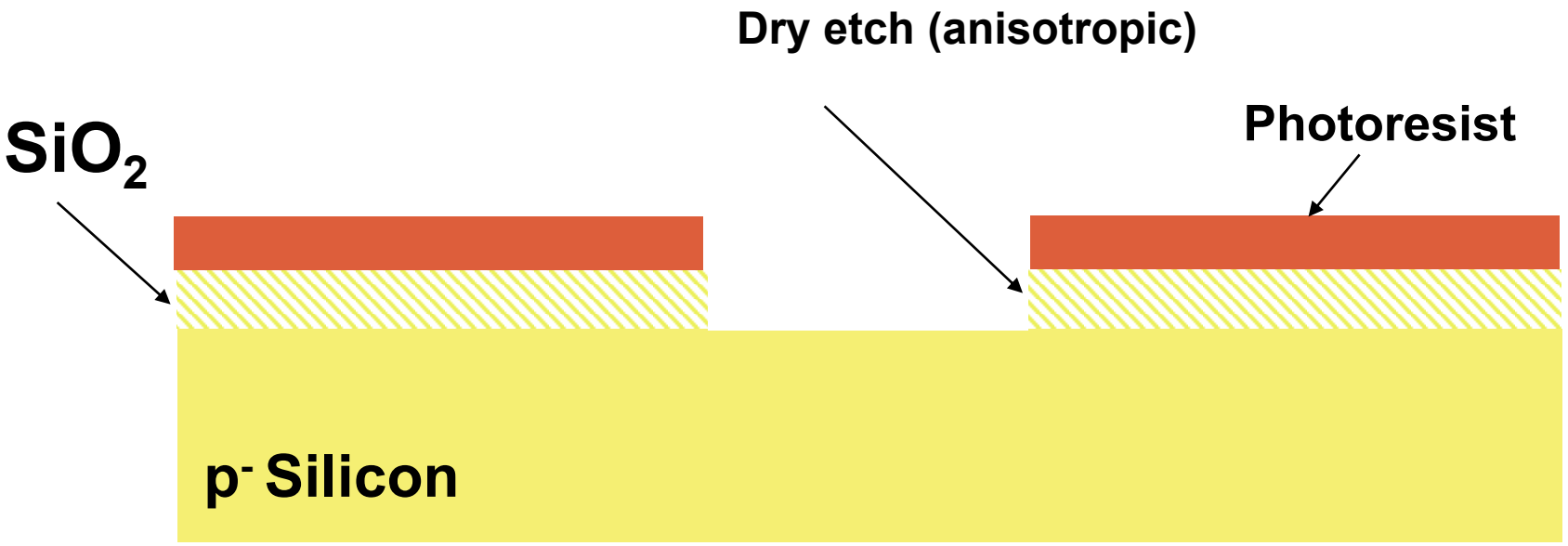
Etching



Desired Physical Features

Note: Vertical Dimensions in silicon generally orders of magnitude smaller than lateral dimensions so different vertical and lateral scales will be used in this discussion. Vertical dimensions of photoresist which is applied on top of wafer is about ½ order of magnitude larger than lateral dimensions

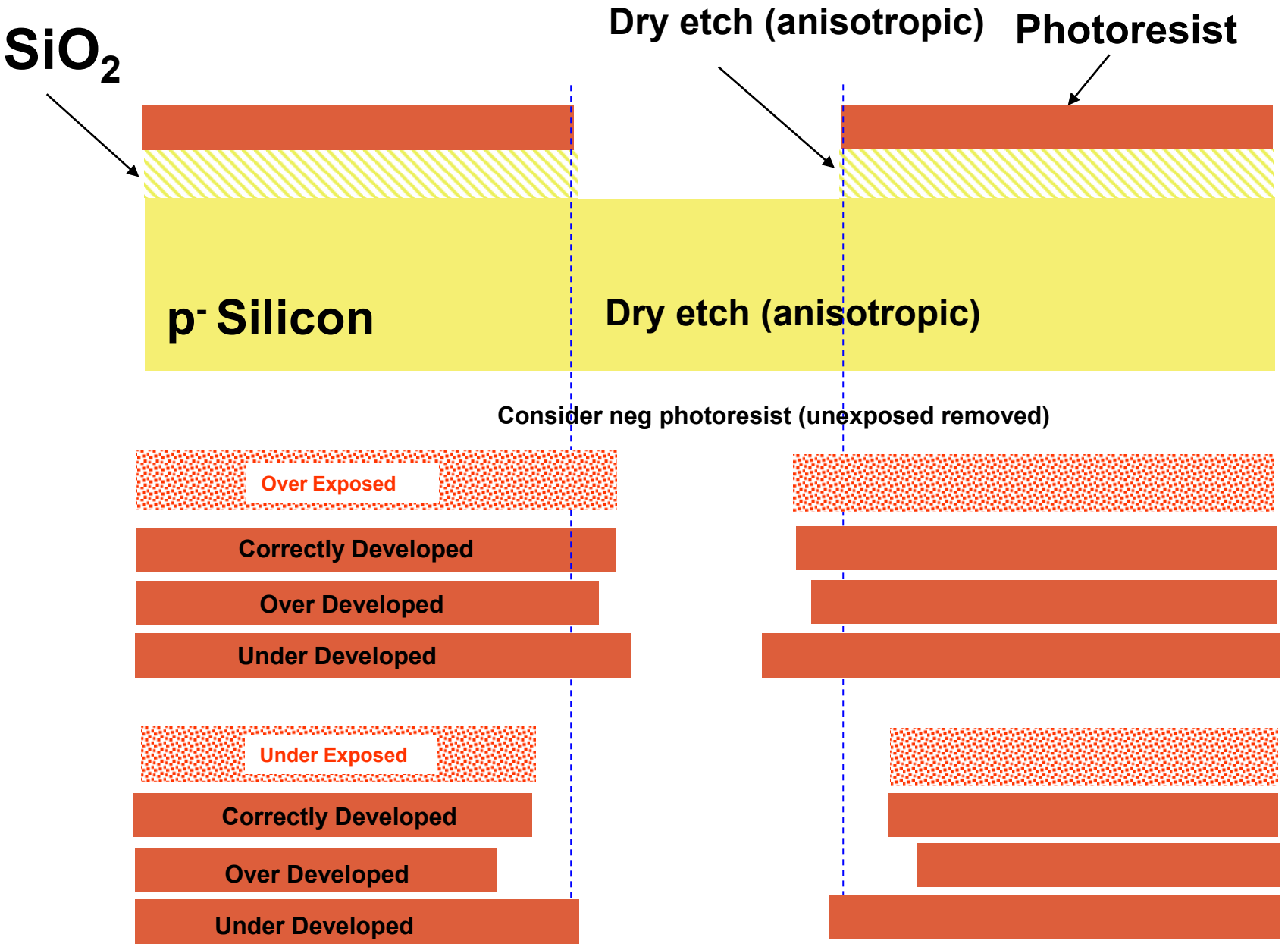
Etching



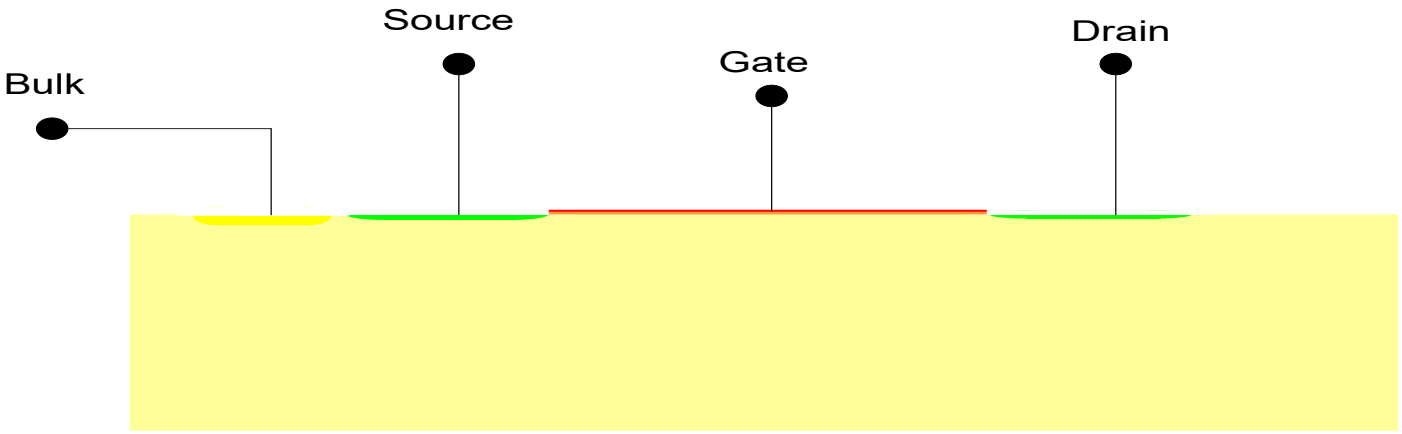
Desired Physical Features

Dry Etch can provide very well-defined and nearly vertical edges (relative to photoresist paterning)

Etching (limited by photolitghographic process)



Lateral Relative to Vertical Dimensions

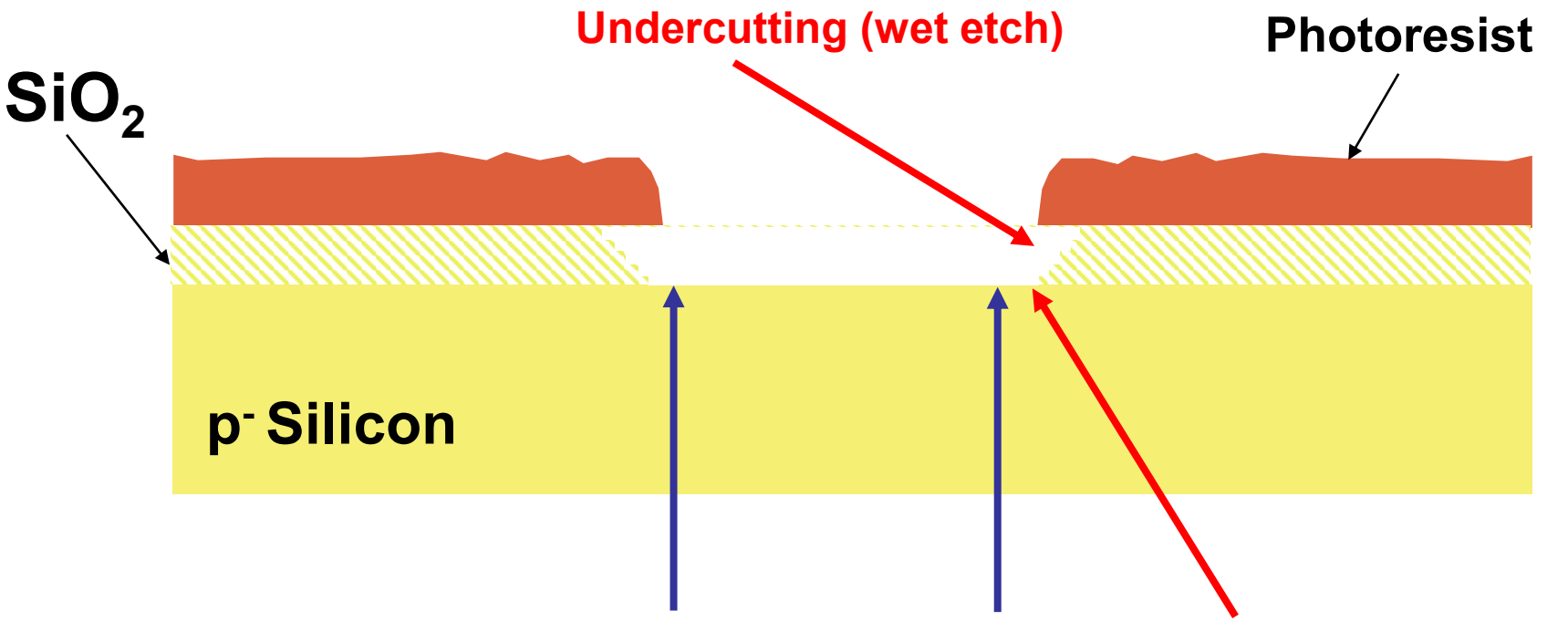


n-channel MOSFET

Still Not to Scale

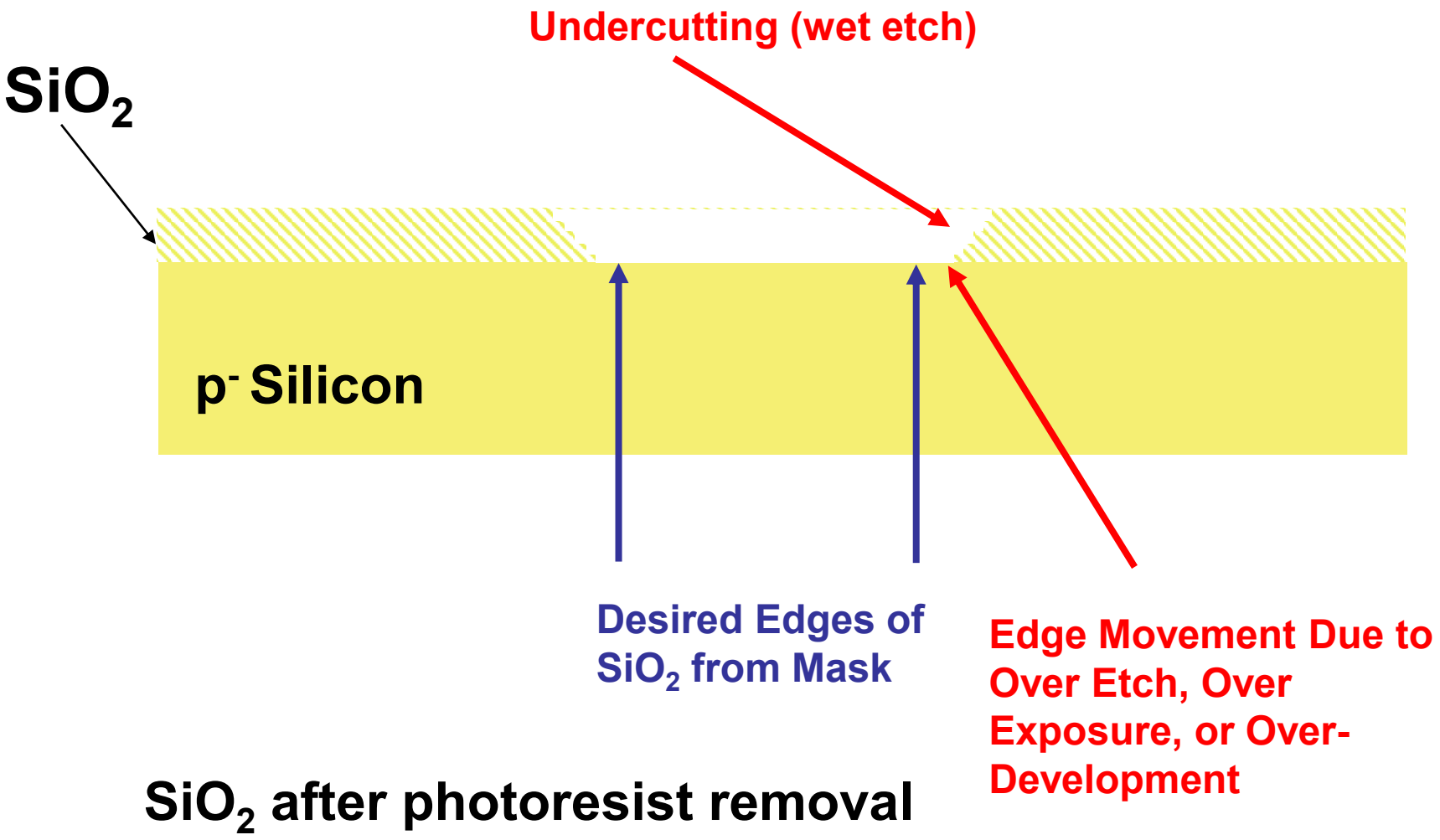
For Example, the wafer thickness is around 250u and the gate oxide is around 50A (5E-3u) and diffusion depths are around λ/5

Etching



Anisotropic etch, Feature Degradation

Etching


Undercutting (wet etch)
SiO_2
p^- Silicon
Desired Edges of SiO_2 from Mask
Edge Movement Due to Over Etch, Over Exposure, or Over-Development
SiO_2 after photoresist removal

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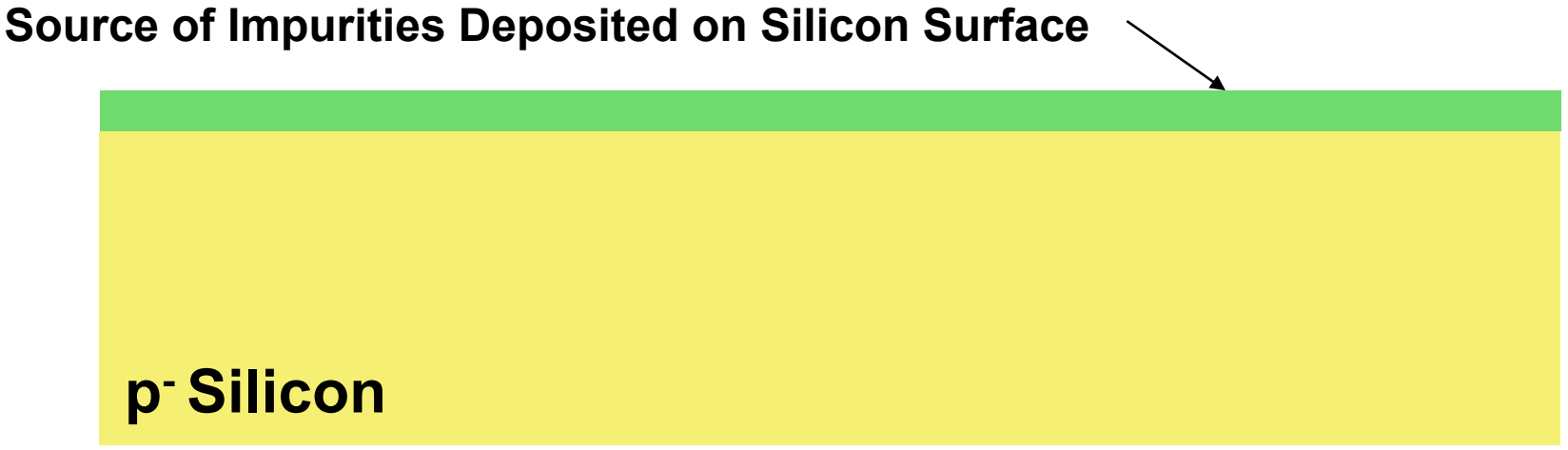
Diffusion

- Controlled Migration of Impurities
  - Time and Temperature Dependent
  - Both vertical and lateral diffusion occurs
  - Crystal orientation affects diffusion rates in lateral and vertical dimensions
  - Materials Dependent
  - Subsequent Movement
  - Electrical Properties Highly Dependent upon Number and Distribution of Impurities
  - Diffusion at 800^{o}C to 1200^{o}C
- Source of Impurities
  - Deposition
  - Ion Implantation
    - Depth depending on ion speed/enery
    - More accurate control of doping levels
    - Fractures silicon crystaline structure during implant
    - Annealing occurs during diffusion
- Types of Impurities
  - n-type Arsenic, Antimony, Phosphorous
  - p-type Gallium, Aluminum, Boron

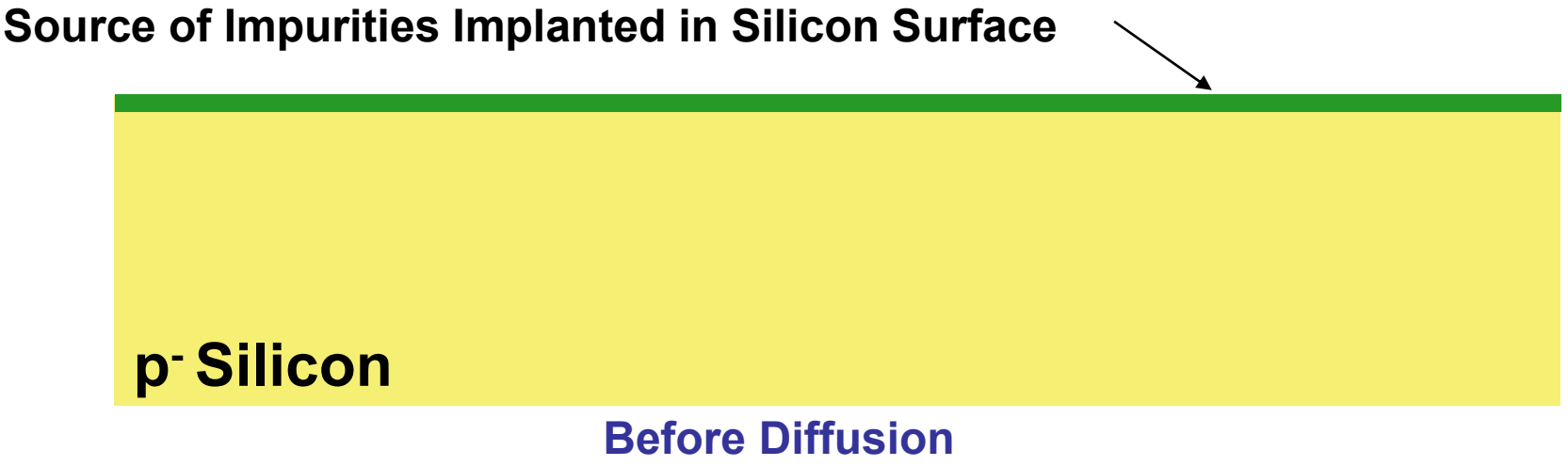
Diffusion



Before Diffusion

After Diffusion

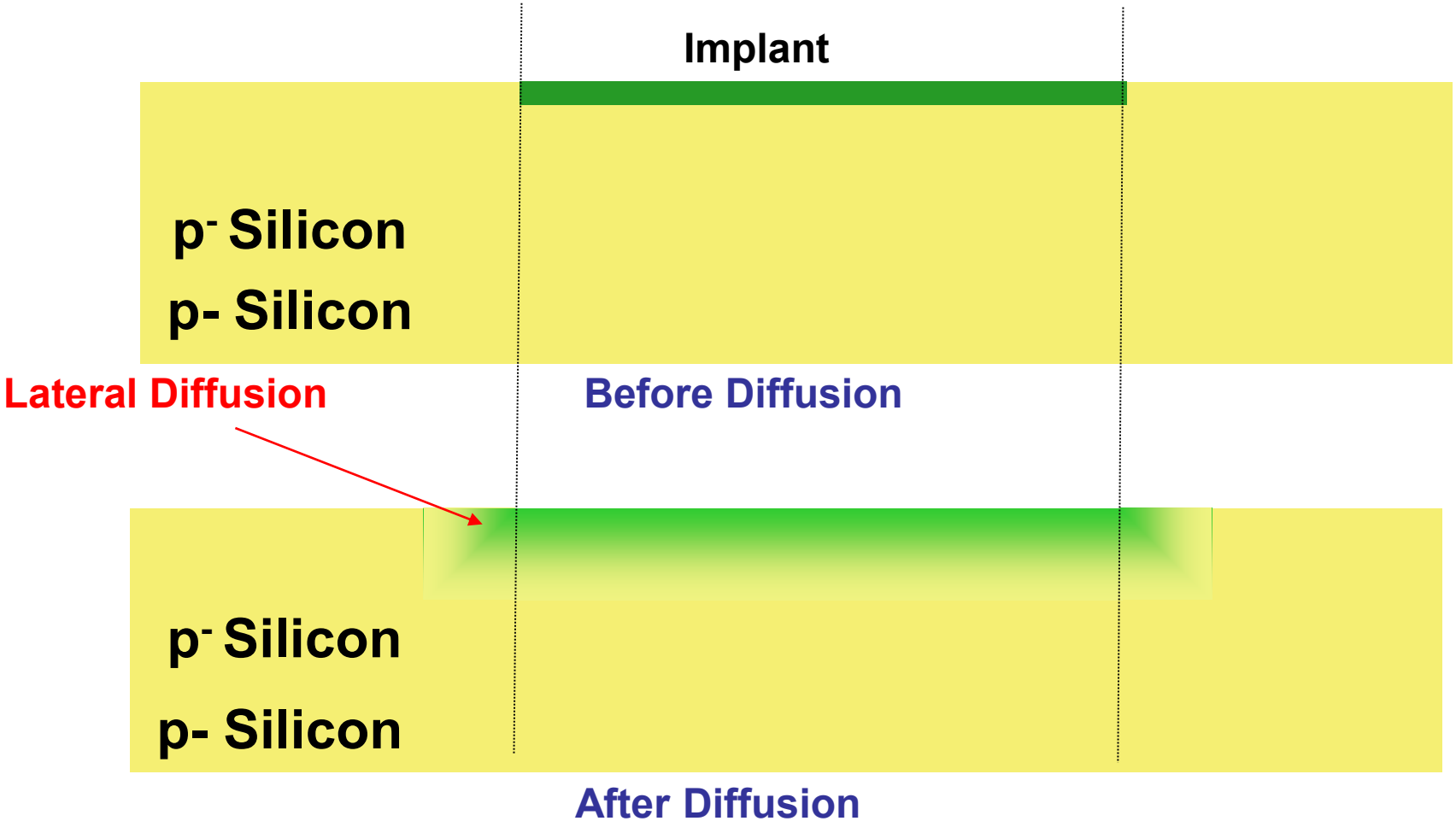
Diffusion



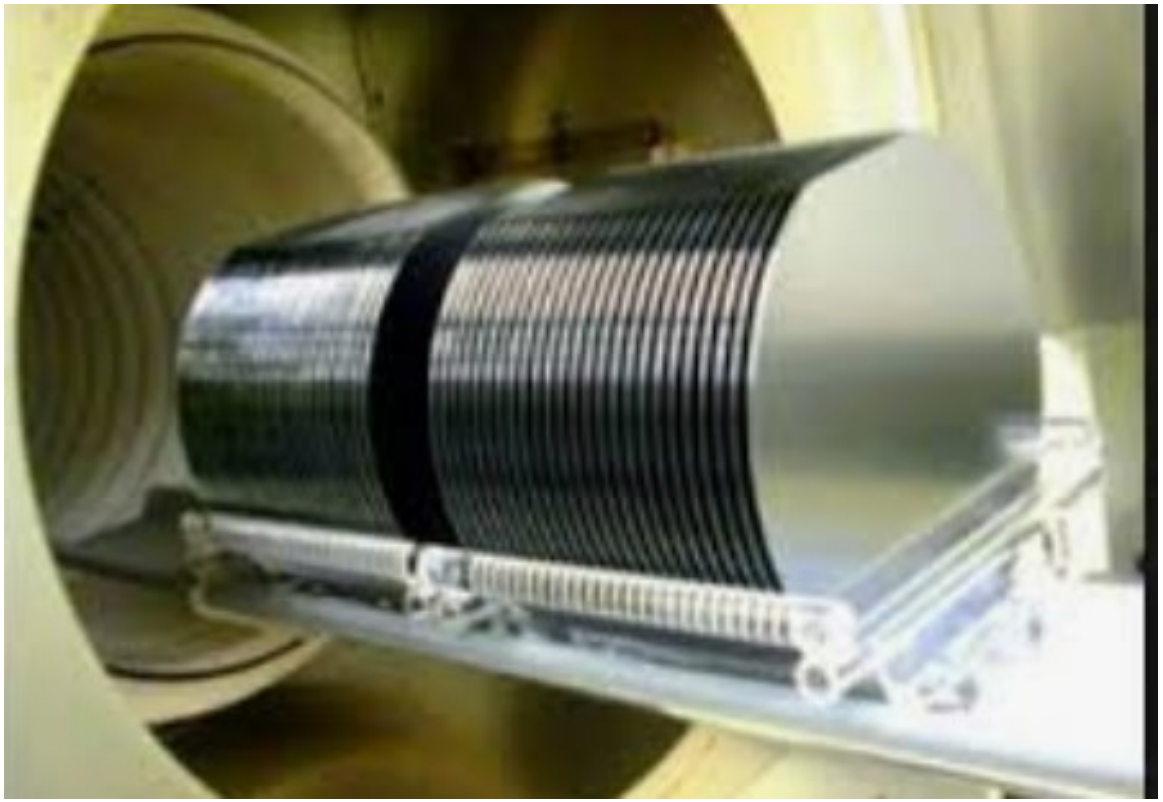
Before Diffusion

After Diffusion

Diffusion

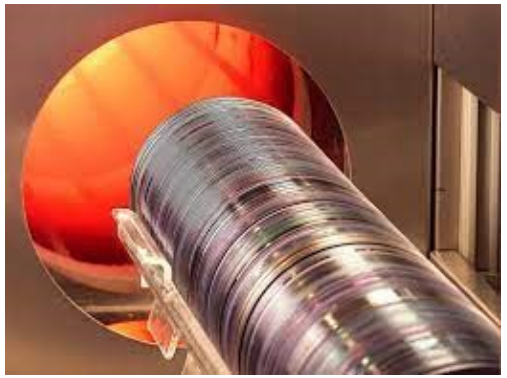

Implant
p- Silicon
p- Silicon
Lateral Diffusion
Before Diffusion
p- Silicon
p- Silicon
After Diffusion

Diffusion



300mm wafers loading in diffusion furnace

Diffusion



Temperature for diffusion of impurities in silicon: 900°C to 1100°C

Time, temperature, uniformity, and time-temperature profile strongly effect properties of semiconductor devices

Melting point of Silicon: 1420°C (Poly around 1414°C)
Melting point of SiO_2: 1710°C
Melting point of Aluminum: 660°C
Melting point of Copper: 1085°C
Melting point of Quartz: 1670°C

Very approximately: diffusion rate targeted at 1um/hour
Very approximately: diffusion depths from 0.5um to 30um

Diffusion rate extremely low (but not 0) at normal operating temperatures

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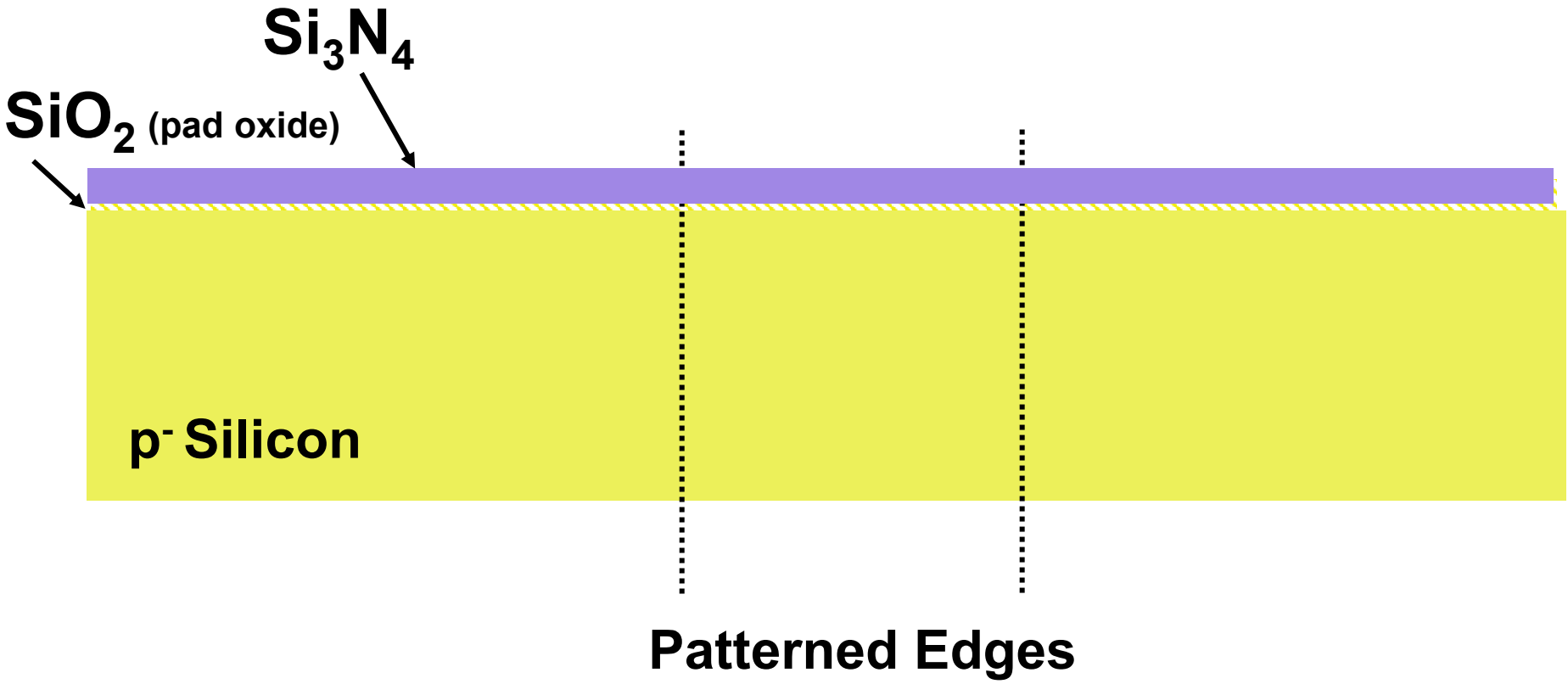
Oxidation

- SiO_2 is widely used as an insulator
  - Excellent insulator properties
- Used for gate dielectric
  - Gate oxide layers very thin
- Used to separate devices by raising threshold voltage
  - termed field oxide
  - field oxide layers very thick
- Methods of Oxidation
  - Thermal Growth (LOCOS)
    - Consumes host silicon
    - x units of SiO_2 consumes .47x units of Si
    - Undercutting of photoresist
    - Compromises planar surface for thick layers
    - Excellent quality
  - Chemical Vapor Deposition
    - Needed to put SiO_2 on materials other than Si

Oxidation

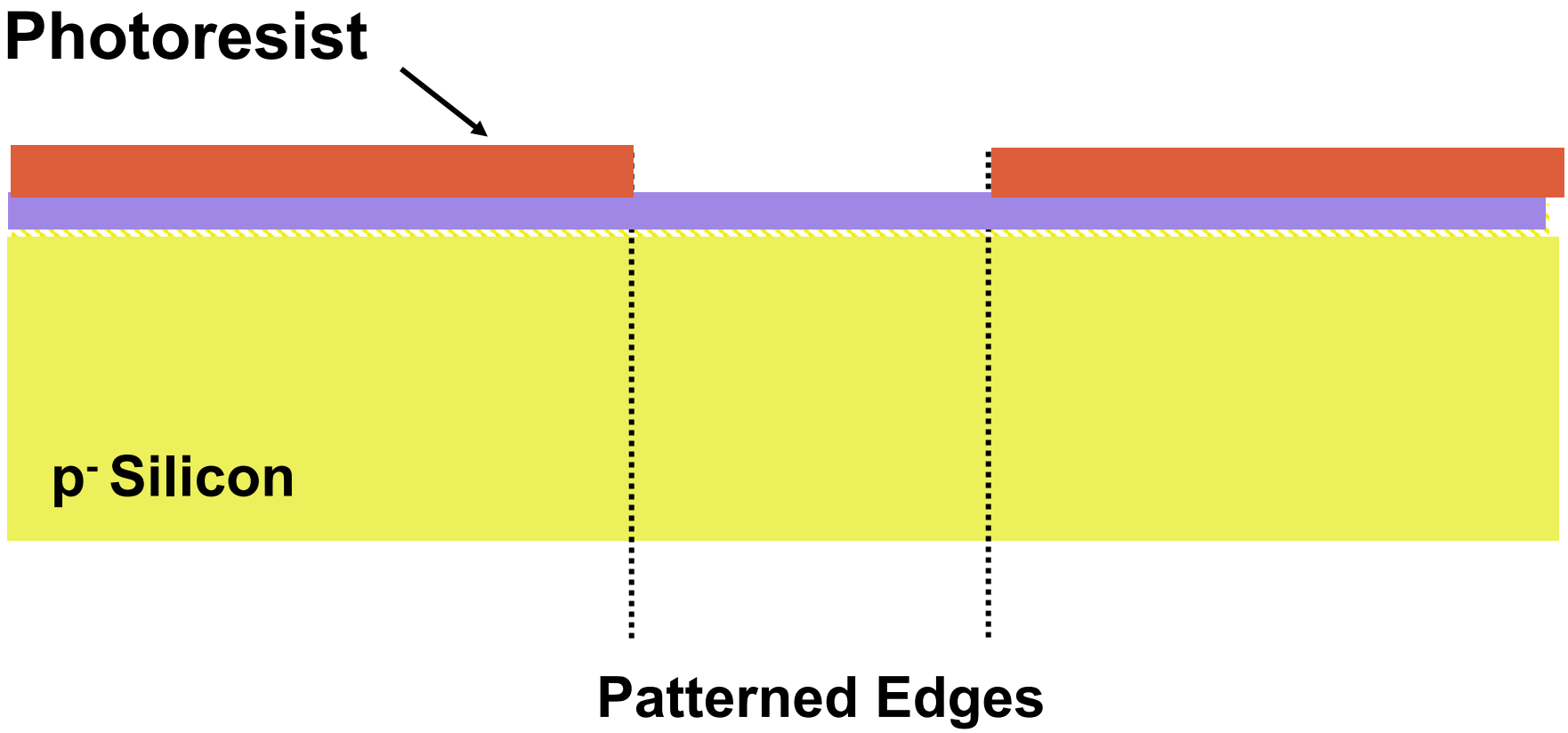
Thin layer of Silicon Nitride is deposited (serves as oxidation barrier)



Thermally Grown SiO_2 (LOCOS) - desired growth

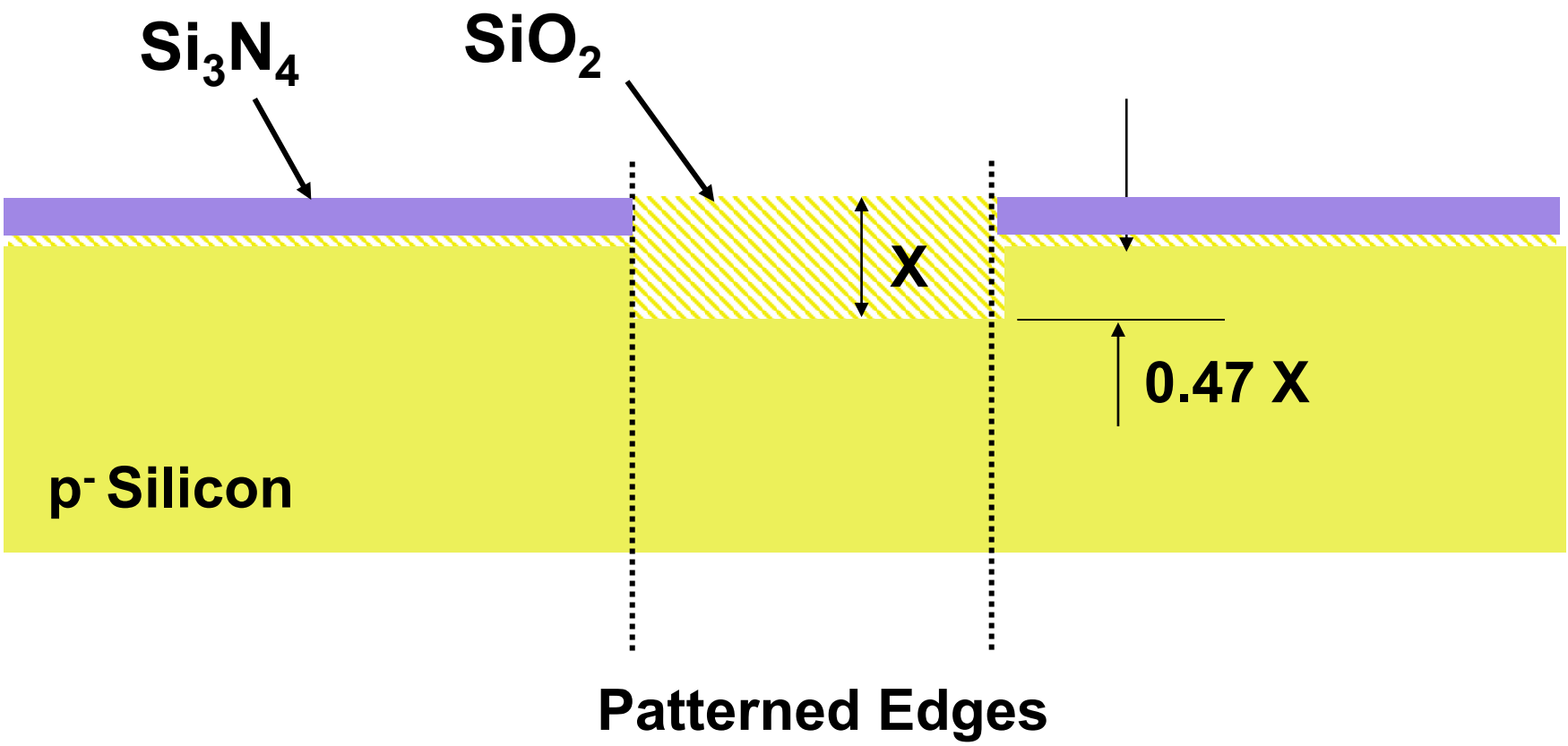
Oxidation

Silicon Nitride Patterned with Photoresist



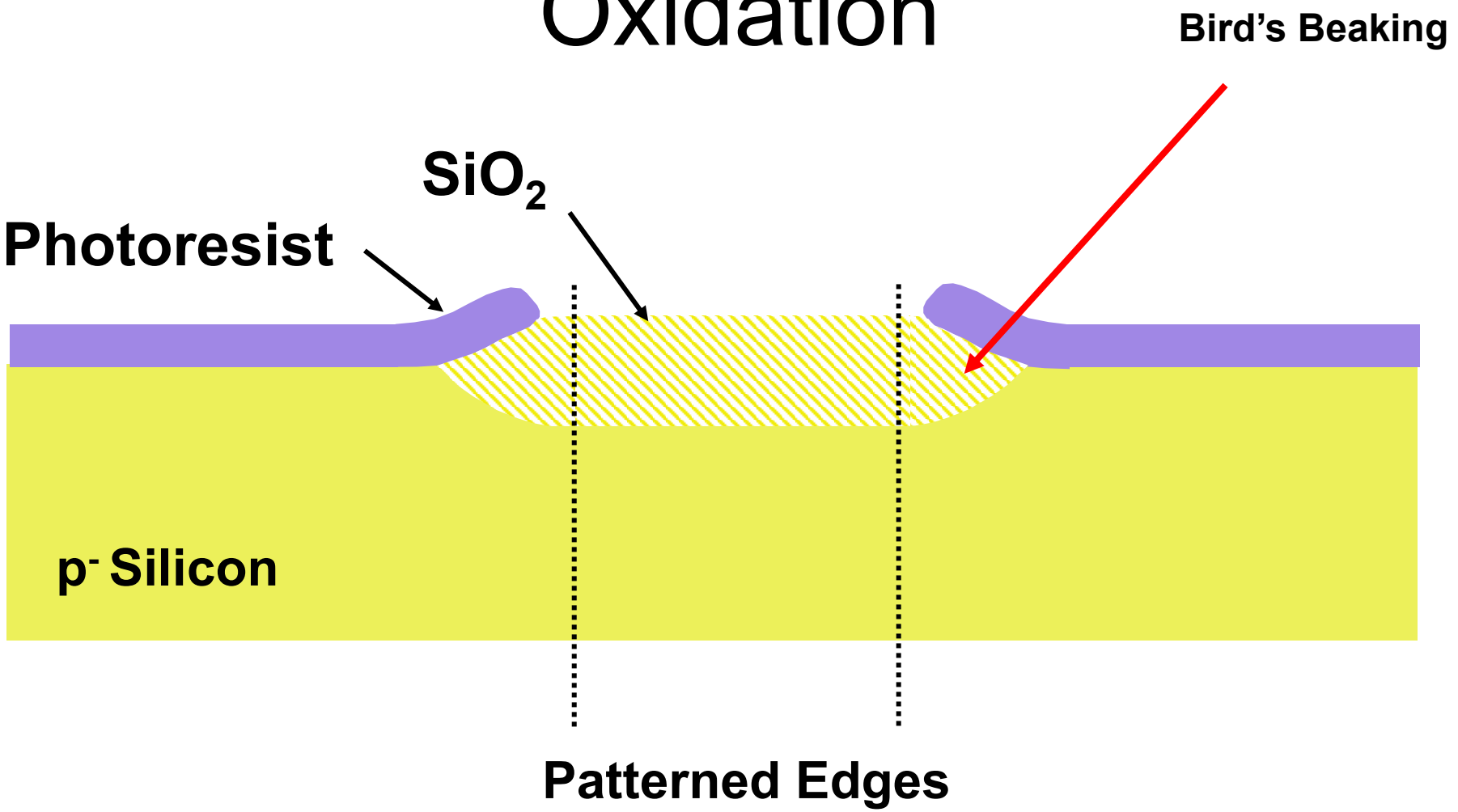
Thermally Grown SiO_2 - desired growth

Oxidation



Thermally Grown SiO_2 - desired growth

Oxidation

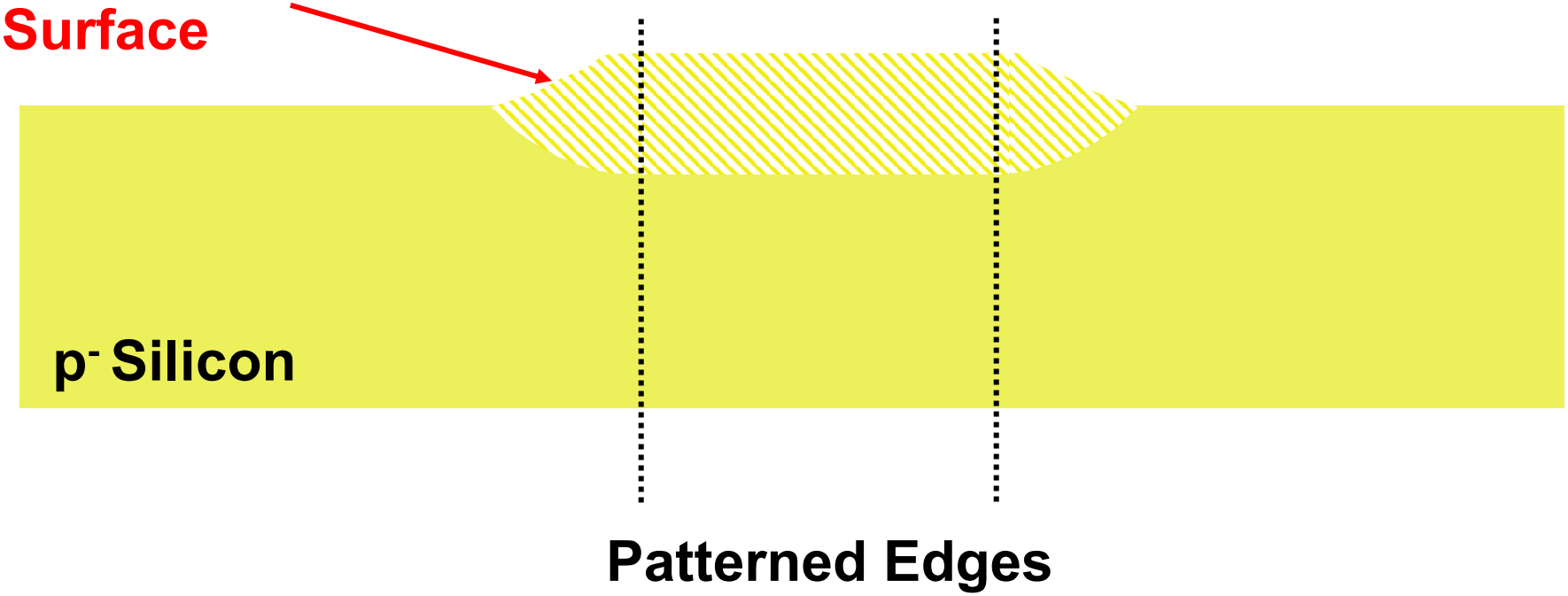


Thermally Grown SiO_2 - actual growth

Oxidation

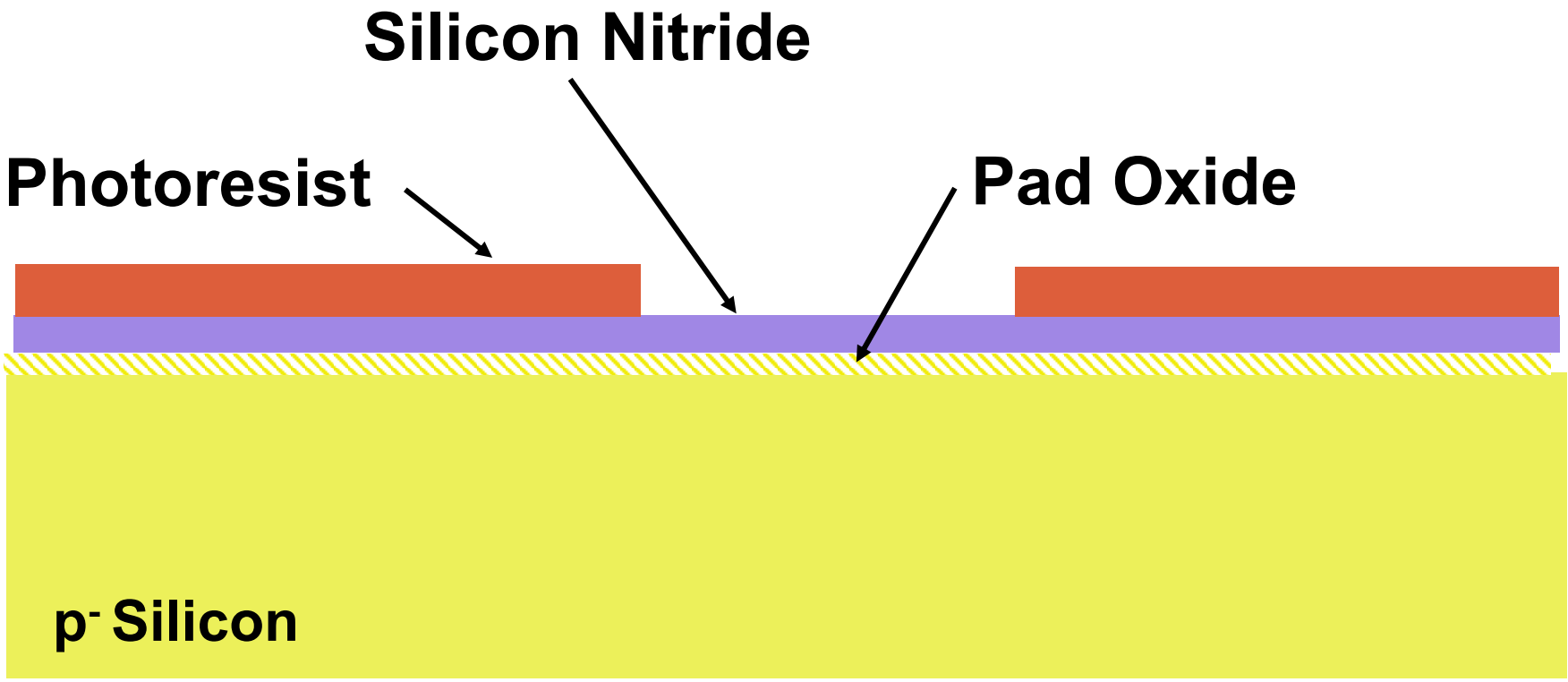
After removal of Si_3N_4

Nonplanar Surface



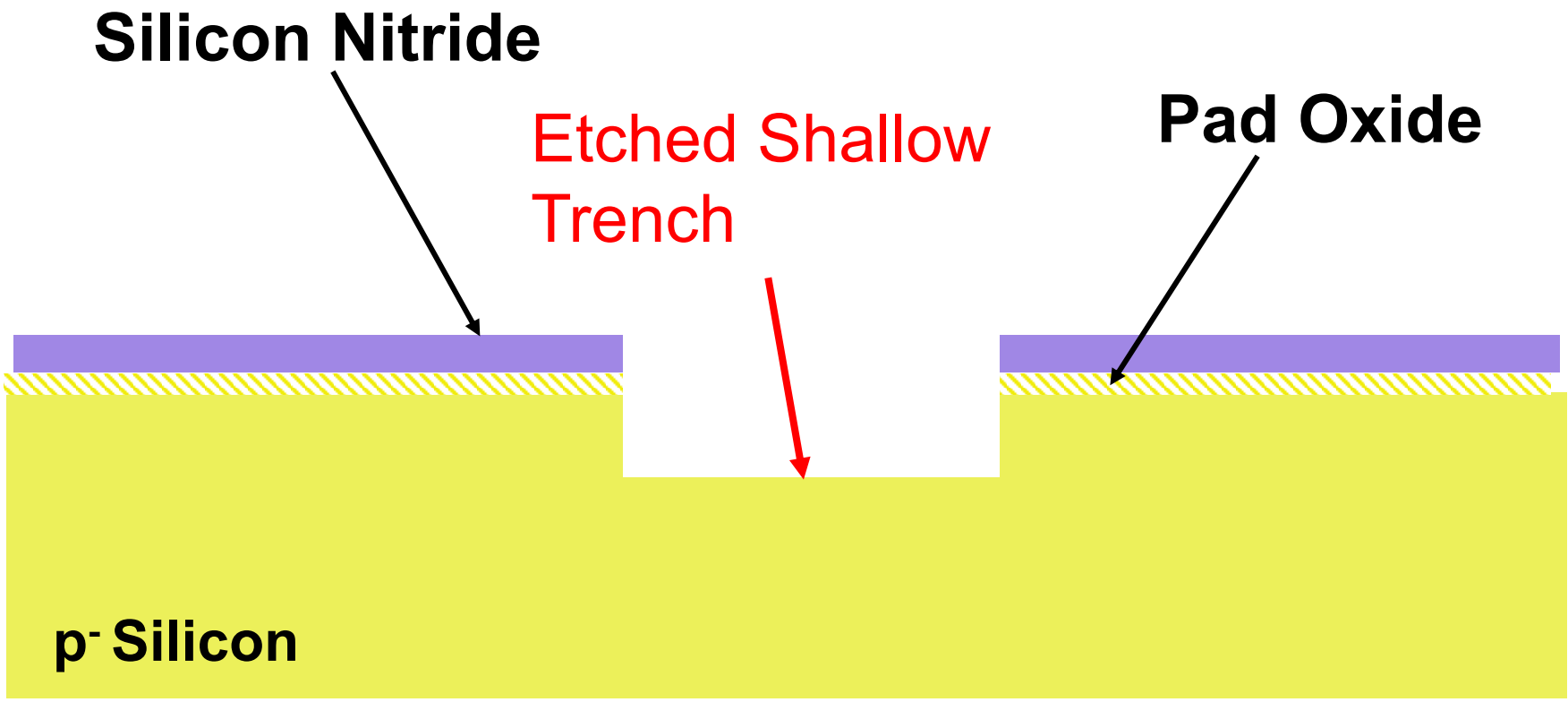
Thermally Grown SiO_2 - actual growth

Oxidation



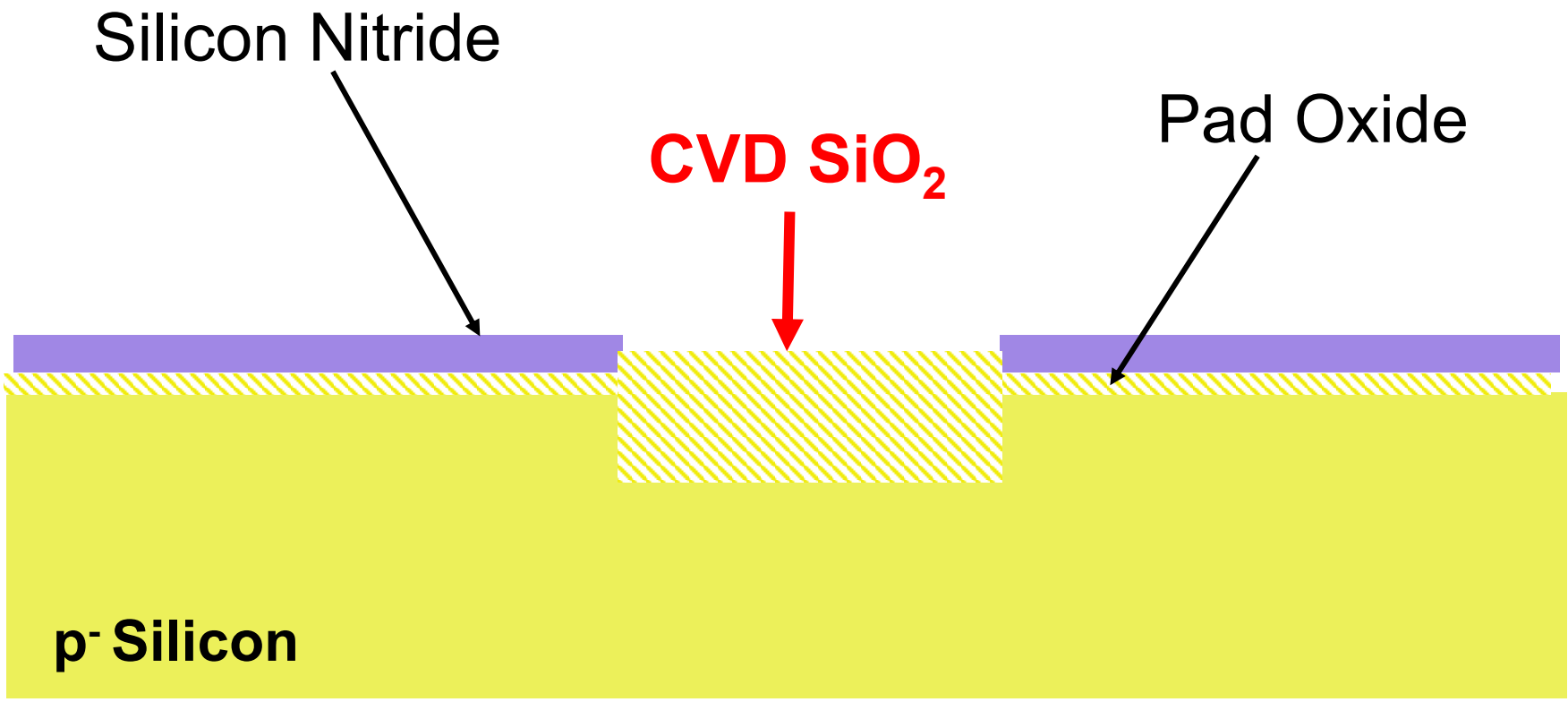
Shallow Trench Isolation (STI)

Oxidation



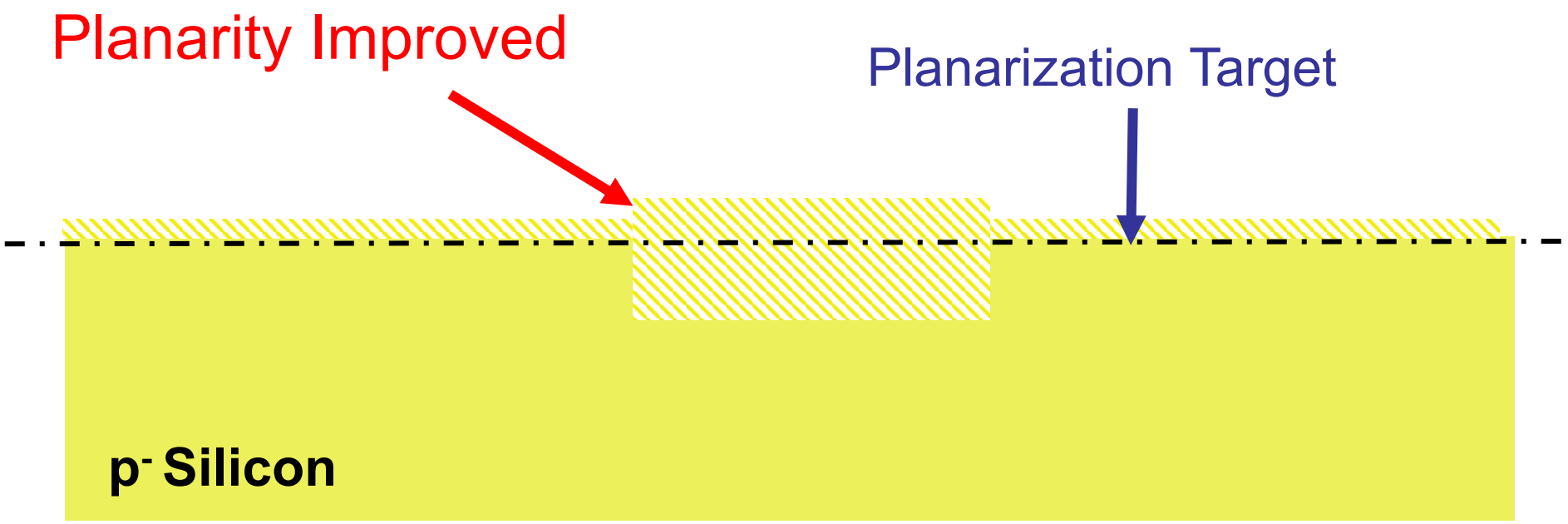
Shallow Trench Isolation (STI)

Oxidation



Shallow Trench Isolation (STI)

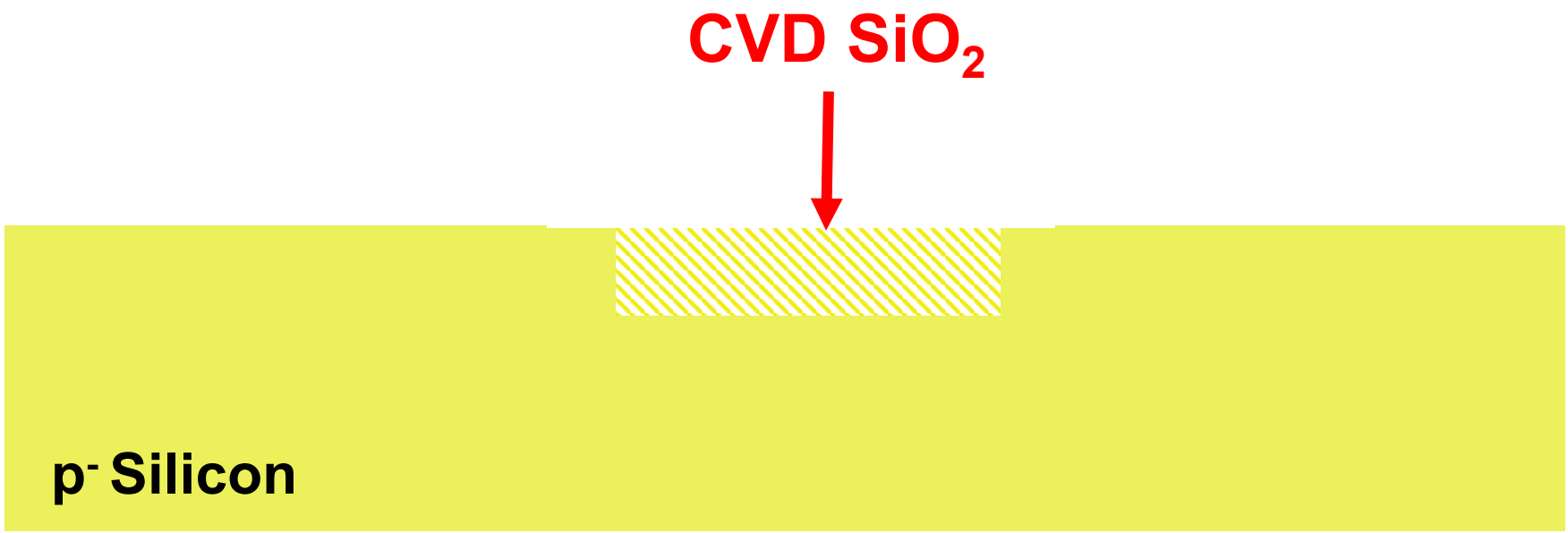
Oxidation



Shallow Trench Isolation (STI)

Oxidation

After Planarization



Shallow Trench Isolation (STI)

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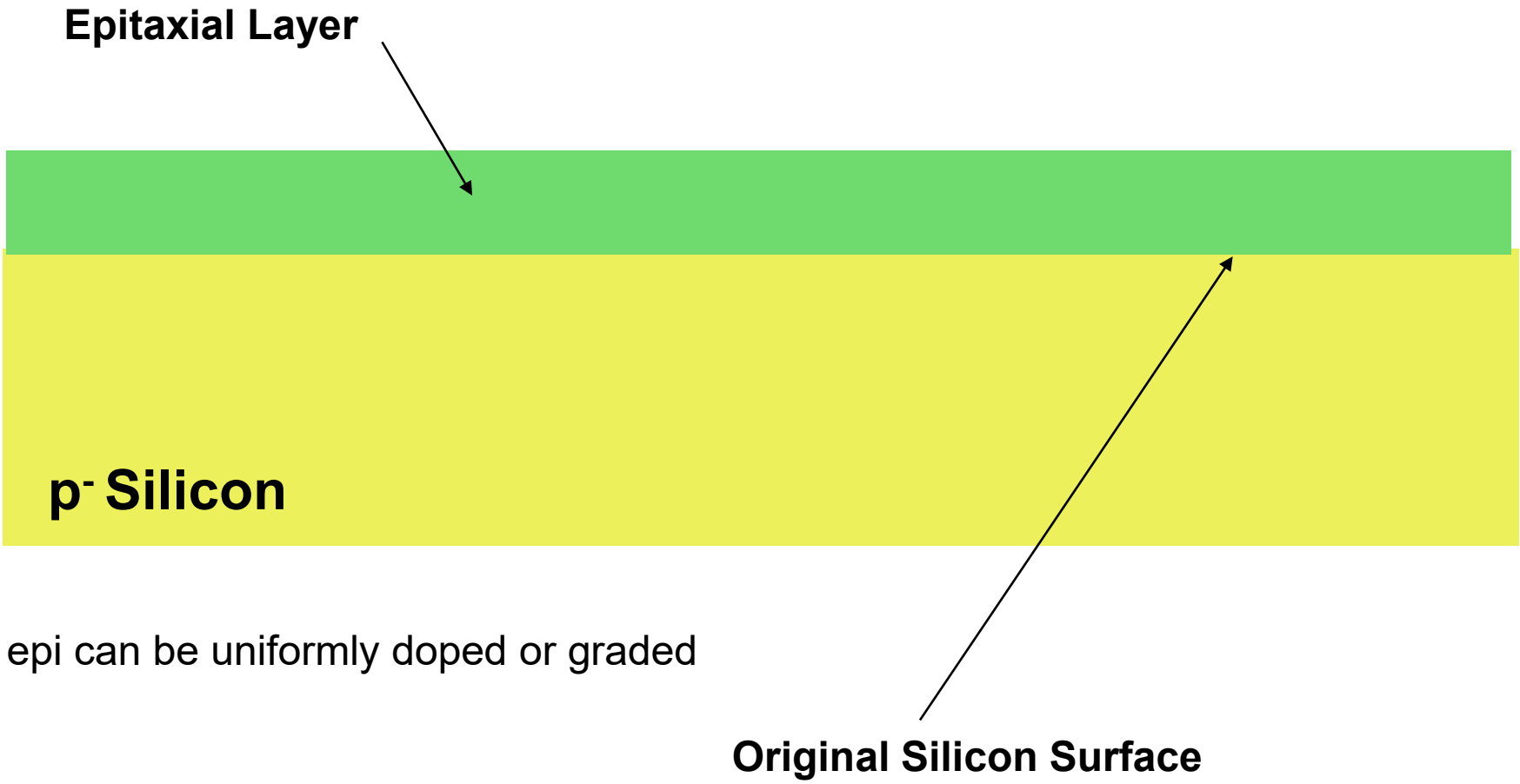
Epitaxy

- Single Crystaline Extension of Substrate Crystal
  - Commonly used in bipolar processes
  - CVD techniques
  - Impurities often added during growth
  - Grows slowly to allow alignmnt with substrate

Epitaxy



epi can be uniformly doped or graded

Question: Why can't a diffusion be used to create the same effect as an epi layer ?

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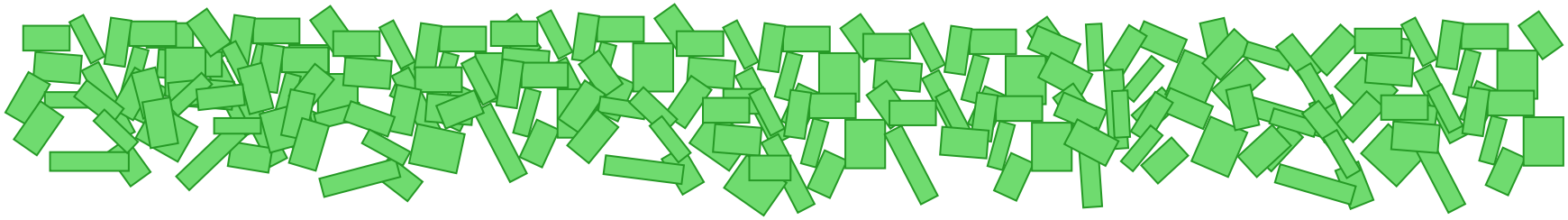
Polysilicon

- Elemental contents identical to that of single crystaline silicon
  - Electrical properties much different
  - If doped heavily makes good conductor
  - If doped moderately makes good resistor
  - Widely used for gates of MOS devices
  - Widely used to form resistors
  - Grows fast over non-crystaline surface
  - Patterned with Photoresist/Etch process
  - Silicide often used in regions where resistance must be small
    - Refractory metal used to form silicide
    - Designer must indicate where silicide is applied (or blocked)

Polysilicon



Polysilicon

Single-Crystaline Silicon

Silicon Wafers and Solar Panels Made from Polysilicon

Where does the silicon come from?

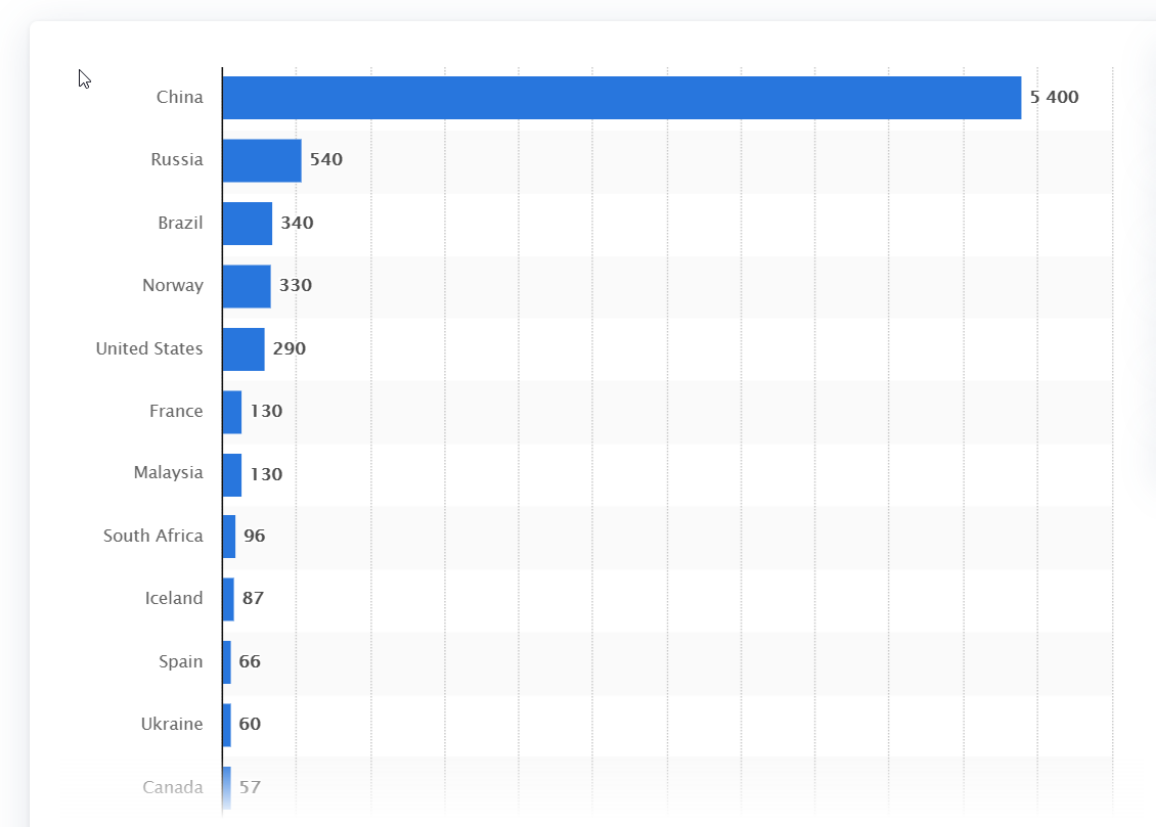
In 2013:

Largest polysilicon producers in 2013 (market-share in %)			
GCL-Poly Energy	China	65,000 tons	22%
Wacker Chemie	Germany	52,000 tons	17%
OCI	South Korea	42,000 tons	14%
Hemlock Semiconductor	USA	36,000 tons	12%
REC	Norway	21,500 tons	7%
Source: Market Realist cites World production capacity at 300,000 tons in 2013.[2] BNEF estimated actual production for 2013 at 227,000 tons[1]			

In 2020:

Major countries in silicon production worldwide in 2020

(in 1,000 metric tons)



In 2020:

The top 10 polysilicon manufacturers for 2020 include:

1. Tongwei (China)
2. Wacker (Germany/United States)
3. Daqo New Energy (China)
4. GCL-Poly (China)
5. Xinte Energy (China)
6. Xingjiang East Hope New Energy (China)
7. OCI (South Korea/Malaysia)
8. Asia Silicon (China)
9. Hemlock (United States)
10. Inner Mongolia Dongli Photovoltaic Electronics (China)

Top 4 projected to be from China by 2022

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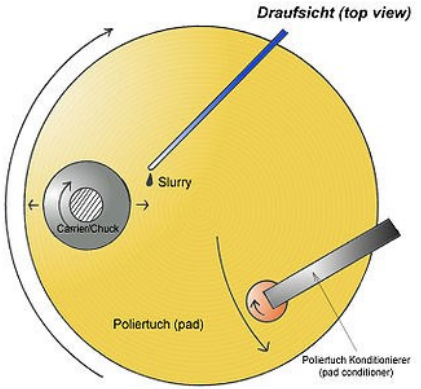
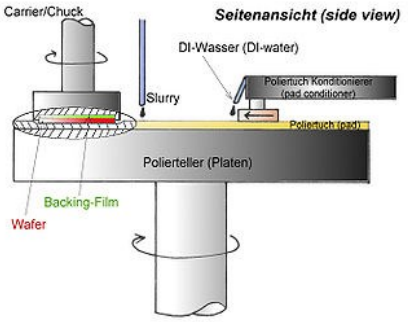
Planarization

- Planarization used to keep surface planar during subsequent processing steps
  - Important for creating good quality layers in subsequent processing steps
  - Mechanically planarized





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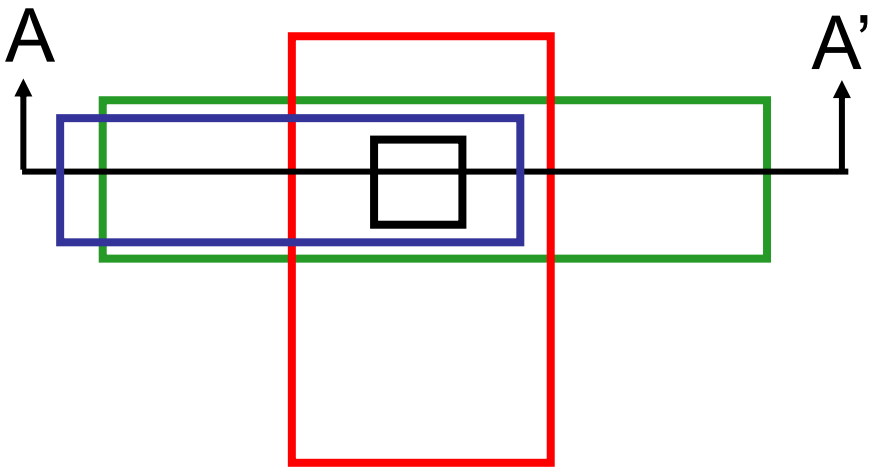
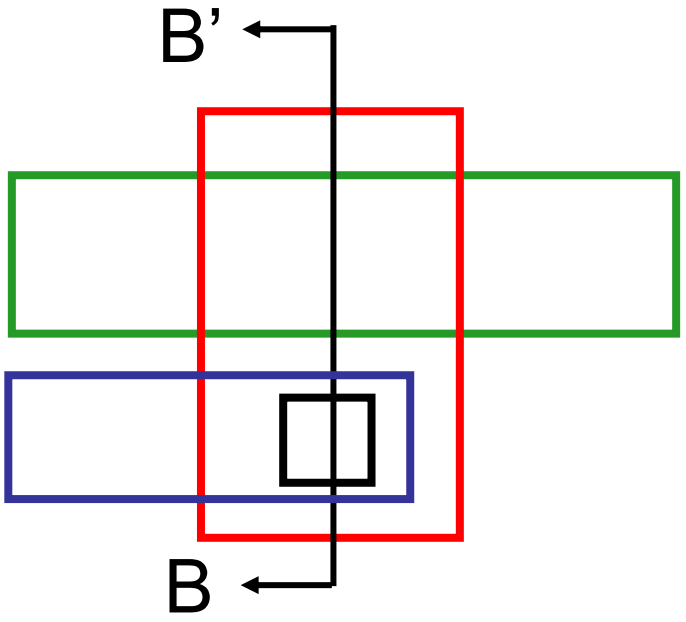
Contacts, Interconnect and Metalization

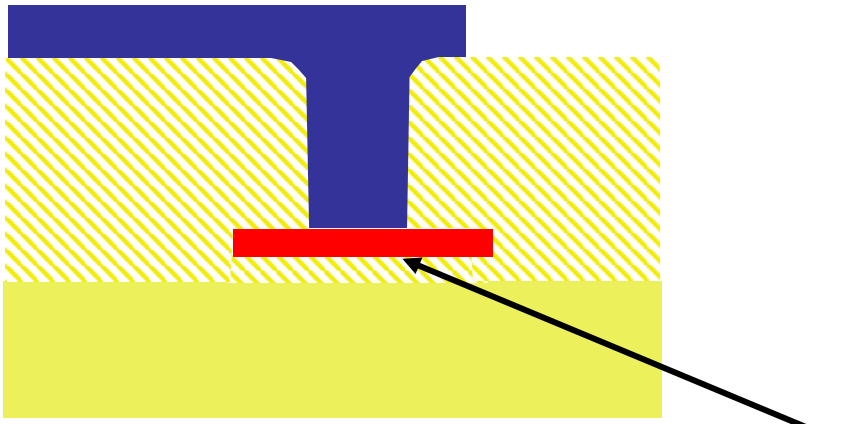
- Contacts usually of a fixed size
  - All etches reach bottom at about the same time
  - Multiple contacts widely used
  - Contacts not allowed to Poly on thin oxide in most processes
  - Dog-bone often needed for minimum-length devices

Contacts





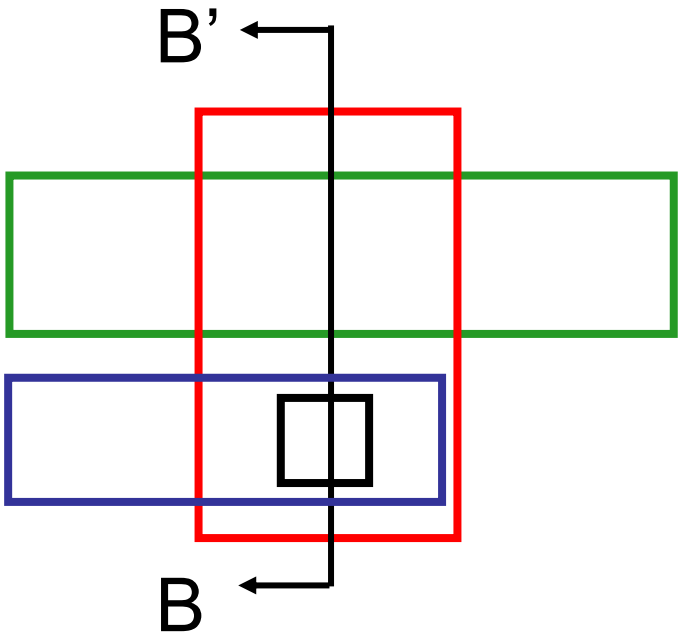
Acceptable Contact

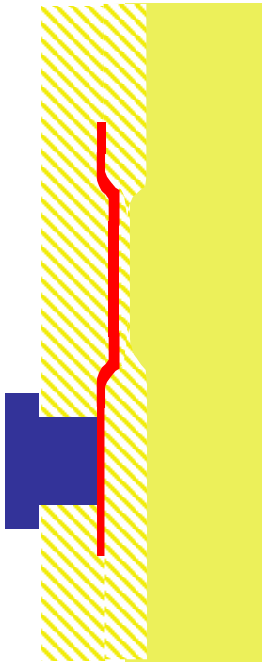


Unacceptable Contact

Vulnerable to pin holes
(usually all contacts are same size)

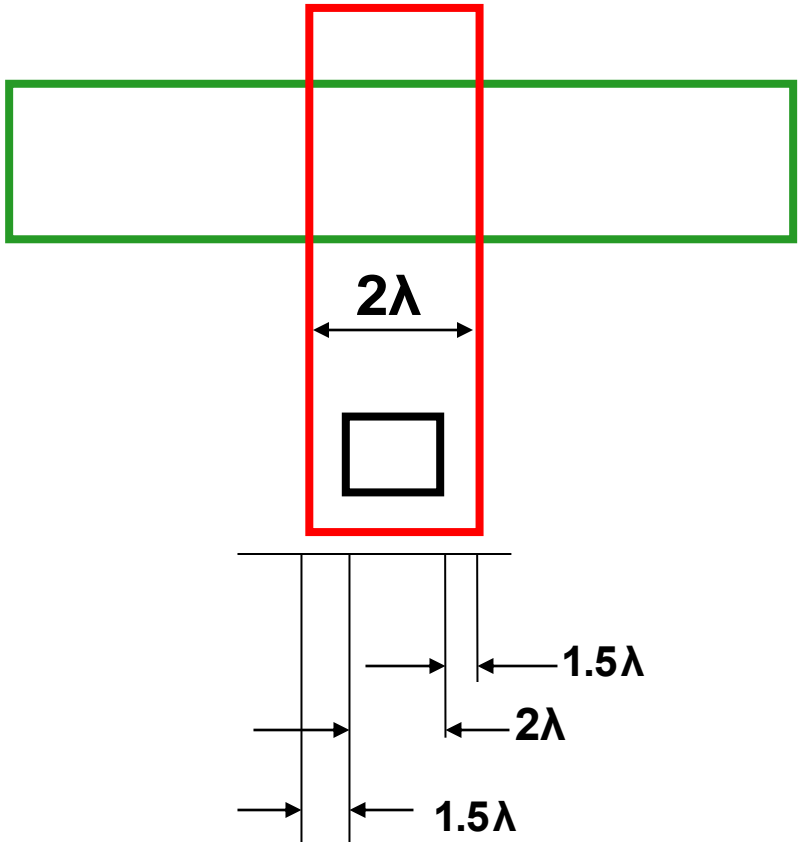
Contacts



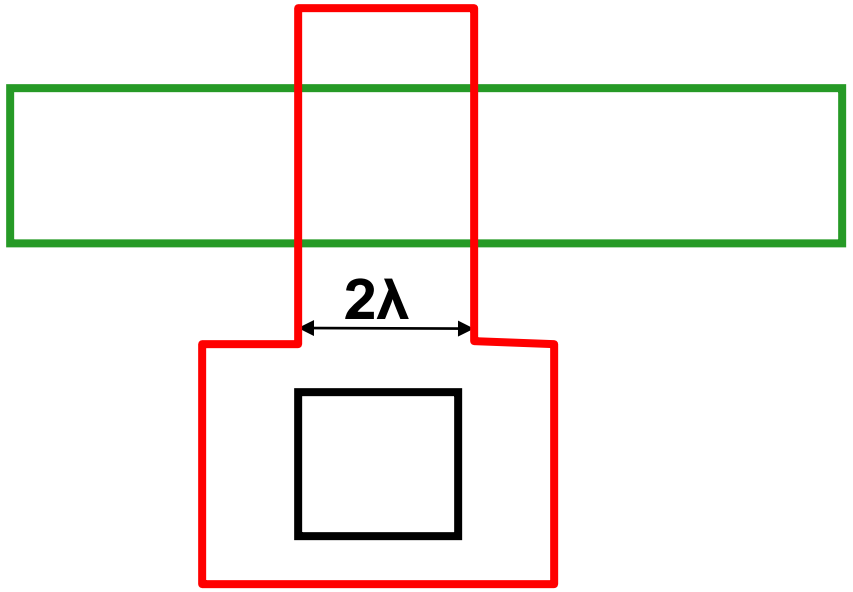


Acceptable Contact

Contacts

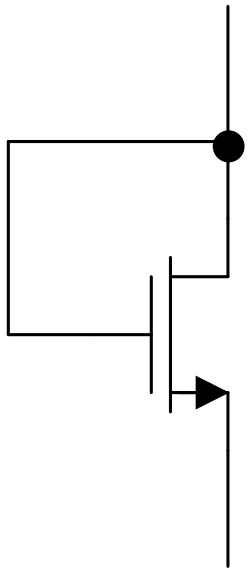


Design Rule Violation

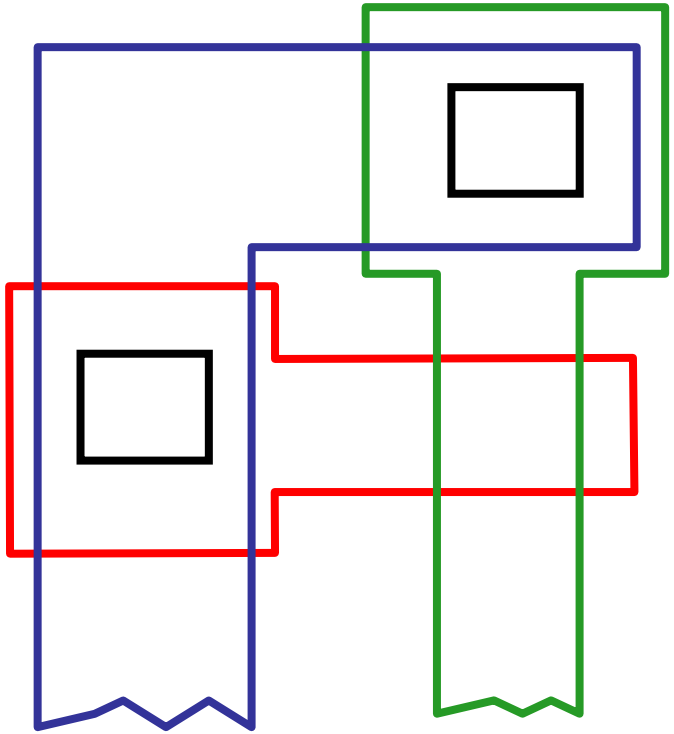


“Dog Bone” Contact

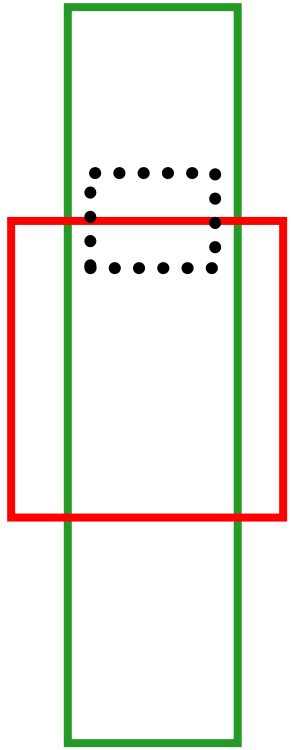
Contacts



Common
Circuit
Connection



Standard Interconnection



Buried Contact

Can save area but not
allowed in many processes

Metalization

- Aluminum widely used for interconnect
- Copper often replacing aluminum in recent processes
- Must not exceed maximum current density
  - around 1ma/u for aluminum and copper
- Ohmic Drop must be managed
- Parasitic Capacitances must be managed
- Interconnects from high to low level metals require connections to each level of metal
- Stacked vias permissible in some processes

Metalization

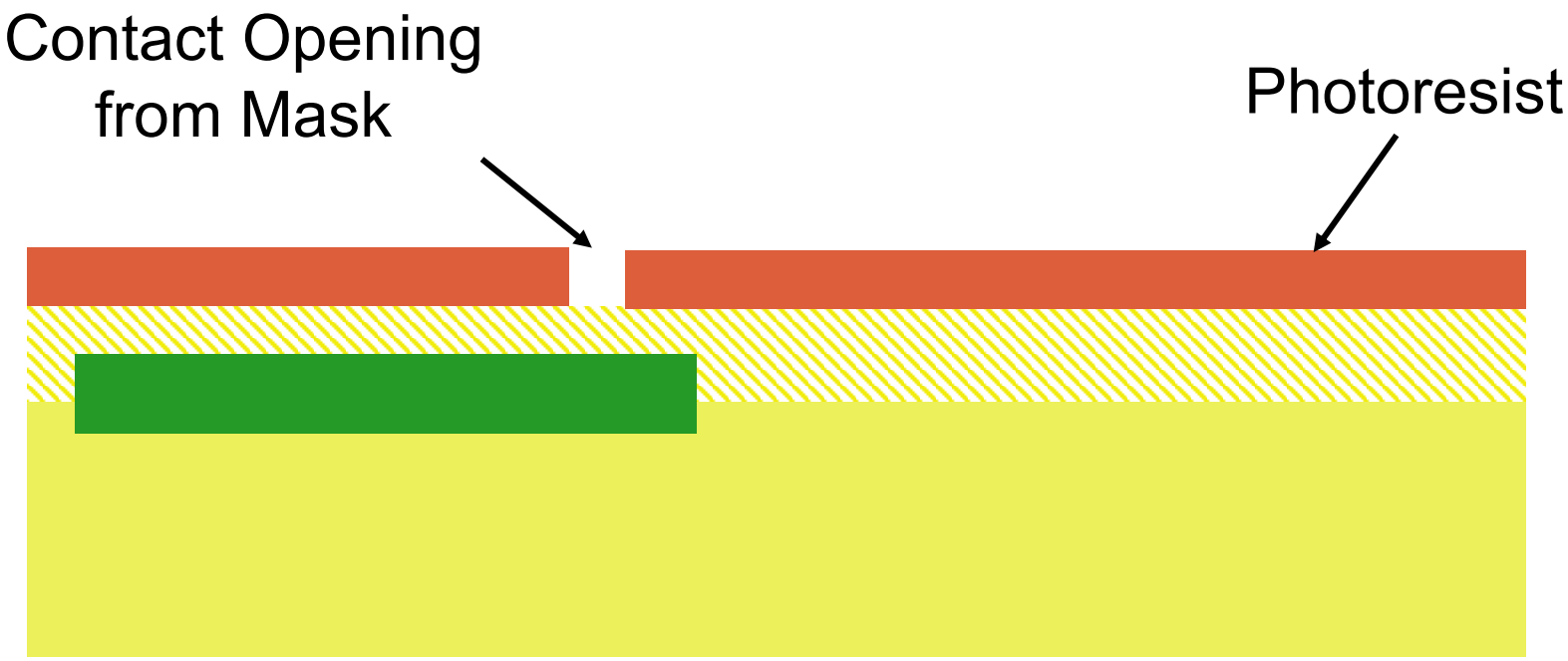
Aluminum

- Aluminum is usually deposited uniformly over entire surface and etched to remove unwanted aluminum
- Mask is used to define area in photoresist where aluminum is to be removed

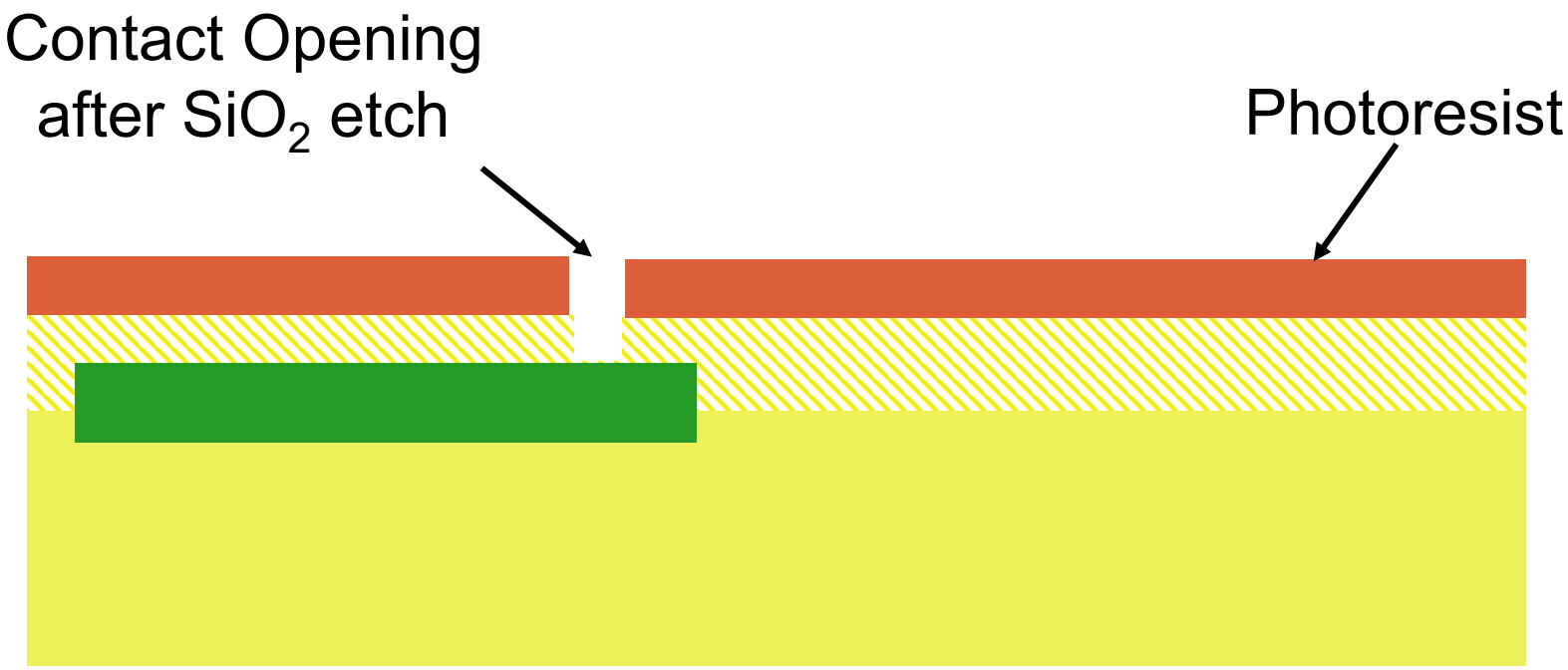
Copper

- Plasma etches not effective at removing copper because of absence of volatile copper compounds
- Barrier metal layers needed to isolate silicon from migration of copper atoms
- Damascene or Dual-Damascene processes used to pattern copper

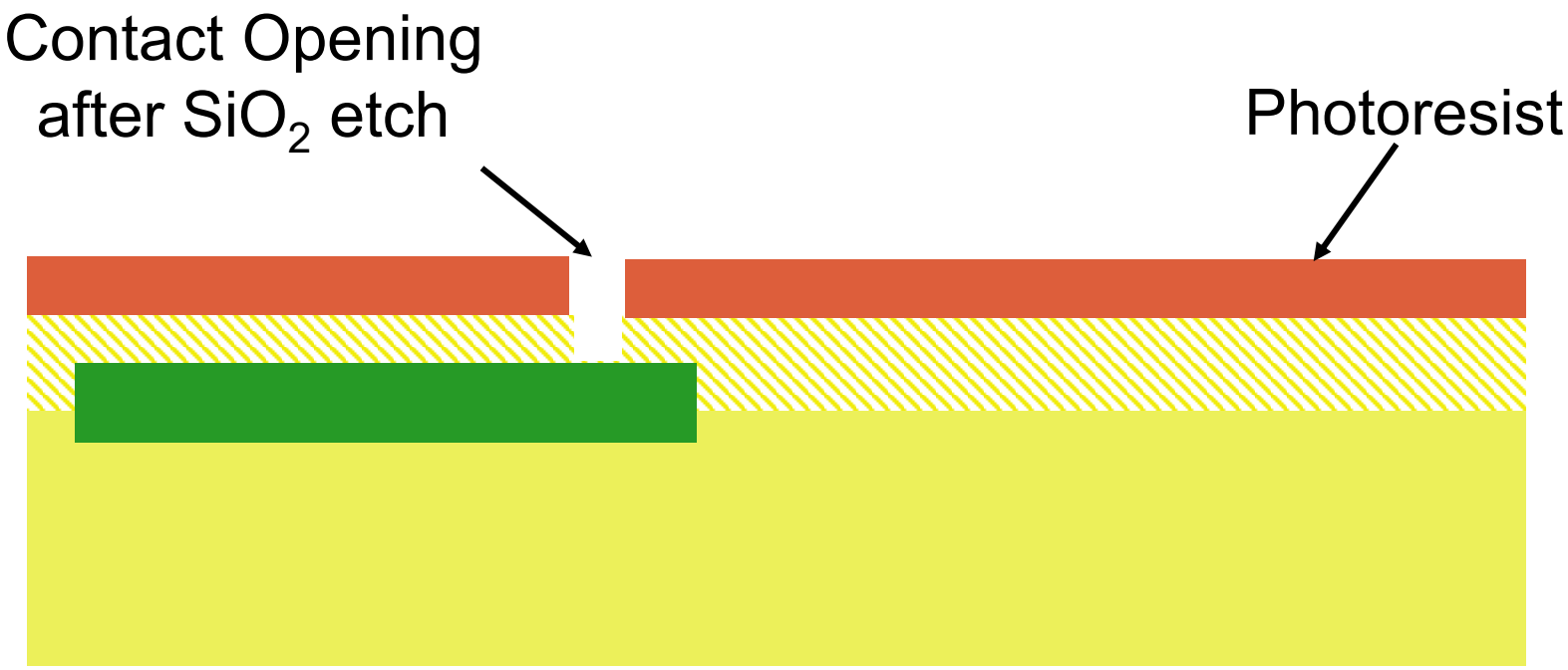
Patterning of Aluminum



Patterning of Aluminum

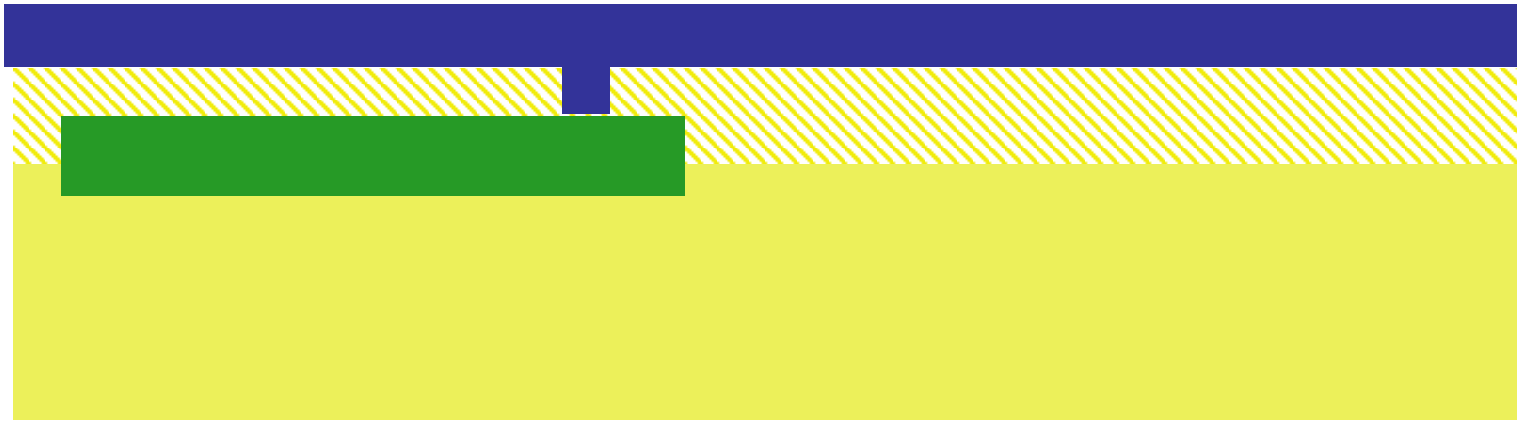


Patterning of Aluminum

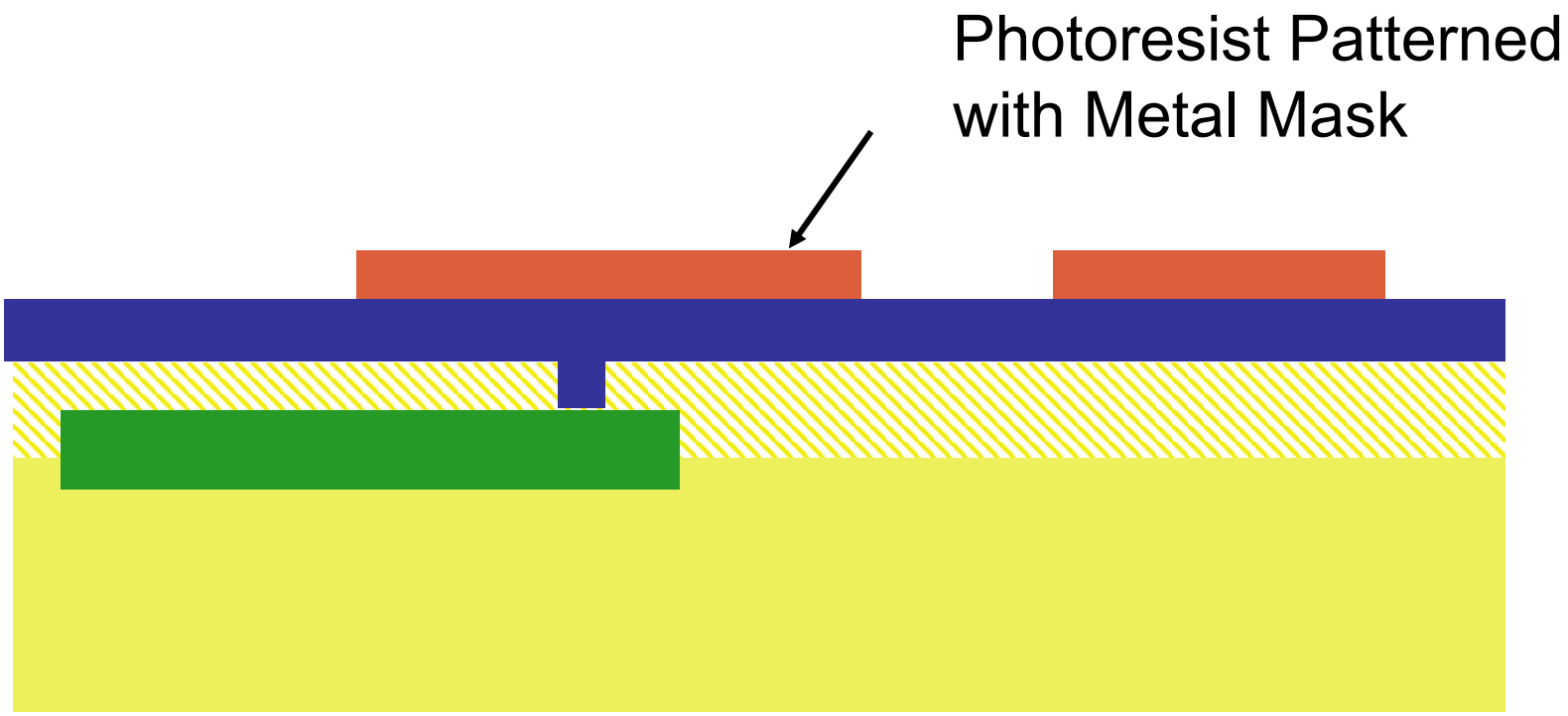


Patterning of Aluminum

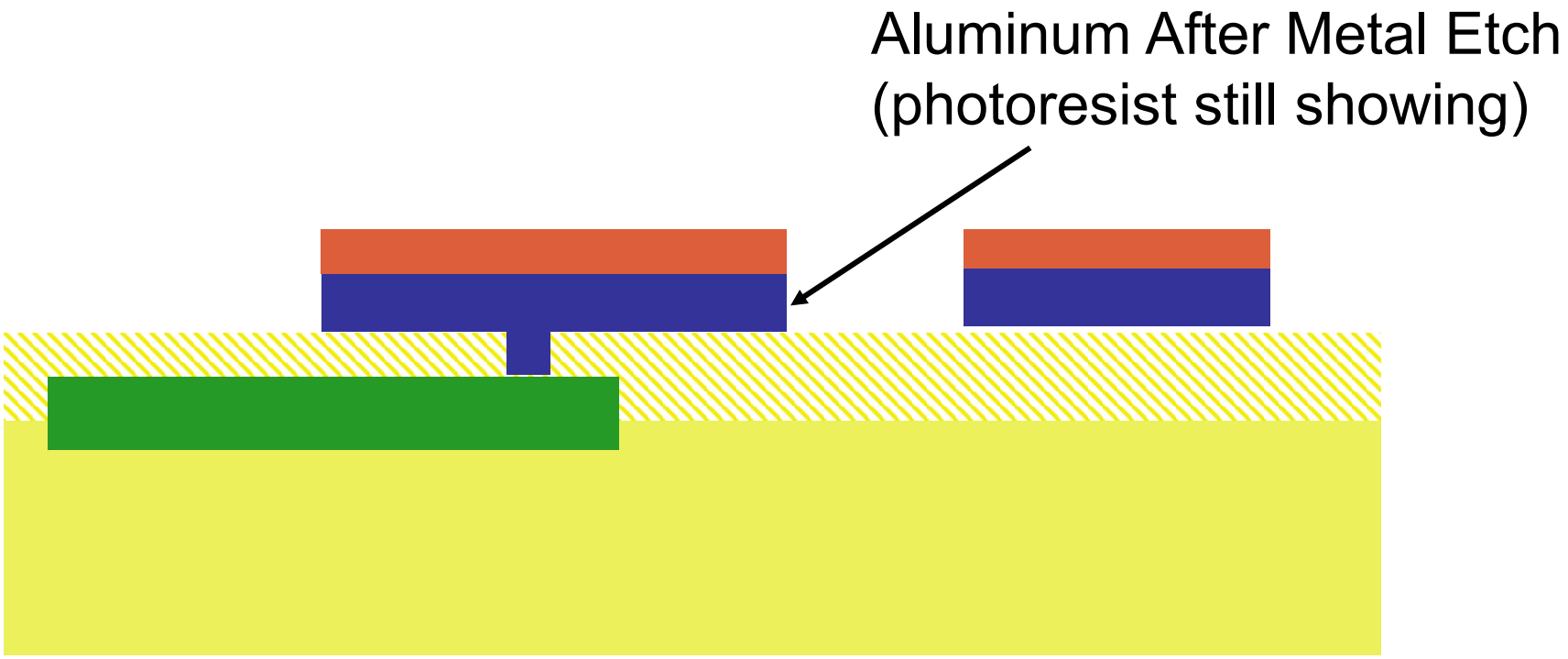
Metal Applied to Entire Surface



Patterning of Aluminum



Patterning of Aluminum



Copper Interconnects

Limitations of Aluminum Interconnects

- Electromigration
- Conductivity not real high

Relevant Key Properties of Copper

- Reduced electromigration problems at given current level
- Better conductivity

Challenges of Copper Interconnects

- Absence of volatile copper compounds (does not etch)
- Copper diffuses into surrounding materials (barrier metal required)

Material	ρ (Ω·m) at 20 °C	σ (S/m) at 20 °C	Temperat coefficient[(K^{-1})
Carbon (graphene)	1.00×10^{-8}	1.00×10^{8}	−0.0002
Silver	1.59×10^{-8}	6.30×10^{7}	0.0038
Copper	1.68×10^{-8}	5.96×10^{7}	0.003862
Annealed copper[note 2]	1.72×10^{-8}	5.80×10^{7}	0.00393
Gold[note 3]	2.44×10^{-8}	4.10×10^{7}	0.0034
Aluminium[note 4]	2.82×10^{-8}	3.50×10^{7}	0.0039
Calcium	3.36×10^{-8}	2.98×10^{7}	0.0041
Tungsten	5.60×10^{-8}	1.79×10^{7}	0.0045
Zinc	5.90×10^{-8}	1.69×10^{7}	0.0037
Nickel	6.99×10^{-8}	1.43×10^{7}	0.006
Lithium	9.28×10^{-8}	1.08×10^{7}	0.006
Iron	9.71×10^{-8}	1.00×10^{7}	0.005
Platinum	1.06×10^{-7}	9.43×10^{6}	0.00392
Tin	1.09×10^{-7}	9.17×10^{6}	0.0045
Carbon steel (1010)	1.43×10^{-7}	6.99×10^{6}	

Source:
Sept 13, 2017

Lead	2.20×10^{-7}	4.55×10^{6}	0.0039
Titanium	4.20×10^{-7}	2.38×10^{6}	0.0038
Grain oriented electrical steel	4.60×10^{-7}	2.17×10^{6}	
Manganin	4.82×10^{-7}	2.07×10^{6}	0.000002
Constantan	4.90×10^{-7}	2.04×10^{6}	0.000008
Stainless steel[note 5]	6.90×10^{-7}	1.45×10^{6}	0.00094
Mercury	9.80×10^{-7}	1.02×10^{6}	0.0009
Nichrome[note 6]	1.10×10^{-6}	6.7×10^{5}	0.0004
GaAs	1.00×10^{-3} to 1.00×10^{8}	1.00×10^{-8} to 10^{3}	
Carbon (amorphous)	5.00×10^{-4} to 8.00×10^{-4}	1.25×10^{3} to 2×10^{3}	−0.0005
Carbon (graphite)[note 7]	2.50×10^{-6} to 5.00×10^{-6} ∥basal plane 3.00×10^{-3} ⊥basal plane	2.00×10^{5} to 3.00×10^{5} ∥basal plane 3.30×10^{2} ⊥basal plane	
PEDOT:PSS	2×10^{-6} to 1×10^{-1}	1×10^{1} to 4.6×10^{5}	?
Germanium[note 8]	4.60×10^{-1}	2.17	−0.048
Sea water[note 9]	2.00×10^{-1}	4.80	
Swimming pool water[note 10]	3.33×10^{-1} to 4.00×10^{-1}	0.25 to 0.30	

Silicon[note 8]	6.40×10^{2}	1.56×10^{-3}	−0.075
Wood (damp)	1.00×10^{3} to 1.00×10^{4}	10^{-4} to 10^{-3}	
Deionized water[note 12]	1.80×10^{5}	5.50×10^{-6}	
Glass	1.00×10^{11} to 1.00×10^{15}	10^{-15} to 10^{-11}	?
Hard rubber	1.00×10^{13}	10^{-14}	?
Wood (oven dry)	1.00×10^{14} to 1.00×10^{16}	10^{-16} to 10^{-14}	
Sulfur	1.00×10^{15}	10^{-16}	?
Air	1.30×10^{14} to 3.30×10^{14}	3×10^{-15} to 8×10^{-15}	
Carbon (diamond)	1.00×10^{12}	$\sim 10^{-13}$	
Fused quartz	7.50×10^{17}	1.30×10^{-18}	?
PET	1.00×10^{21}	10^{-21}	?
Teflon	1.00×10^{23} to 1.00×10^{25}	10^{-25} to 10^{-23}	?

Stay Safe and Stay Healthy !

End of Lecture 10